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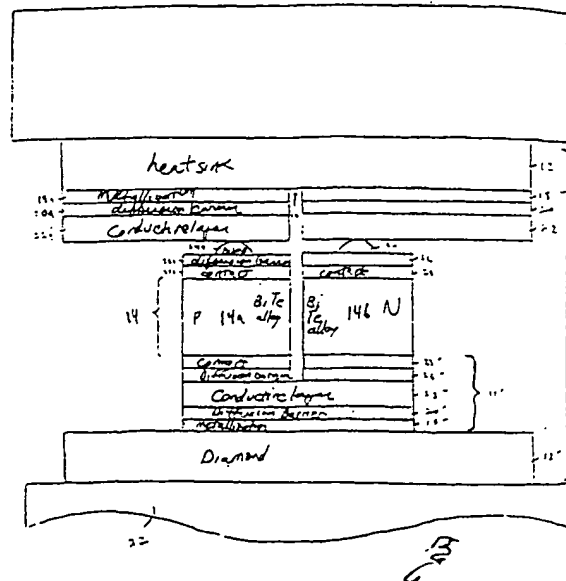
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(71) Applicant (for all designated States except US): CALIFORNIA INSTITUTE OF TECHNOLOGY [US/US]; 1200 East California Boulevard, Mail Code 201-85, Pasadena, CA 91125 (US).		(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).	
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(54) Title: MICROFABRICATED THERMOELECTRIC POWER-GENERATION DEVICES

(57) Abstract

A device (10) for generating power to run an electronic component. The device includes a heat-conducting substrate (12, 12') (composed, e.g., of diamond or another high thermal conductivity material) disposed in thermal contact with a high temperature region (13). During operation, heat flows from the high temperature region (13) into the heat-conducting substrate (12) from which the heat flows into the electrical power generator (10). A thermoelectric material (14) (e.g., a BiTe alloy-based film or other thermoelectric material) is placed in thermal contact with the heat-conducting substrate (12, 12'). A low temperature region (27) is located on the side of the thermoelectric material opposite that of the high temperature region (13). The thermal gradient generates electrical power and drives an electrical component.



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MICROFABRICATED THERMOELECTRIC POWER-GENERATION DEVICES

Field of the Invention

5 This invention relates to devices employing a micro-sized thermoelectric power generating device.

Cross Reference To Related Applications

 This application claims the benefit of the U.S.
10 Provisional Application No. 60/095,829 filed on August 7, 1998, and U.S. Provisional Application Serial No. 60,096,657 filed on August 13, 1998, which are incorporated herein by reference.

15 Statement as to Federally Sponsored Research

 The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 U.S.C. 202) in which the Contractor has elected to retain title.

20

Background

 Small electronic devices, such as those using integrated circuits, continue to play a major role in all aspects of society. Batteries have traditionally been used to power such
25 devices.

 The energy in a battery dissipates over time, requiring battery replacement or recharging.

Portable devices can be powered using thermoelectric ("TE") effects. The thermoelectric material generates power based on a thermal gradient. The thermal gradient for a wristwatch may be created by one side of the watch being exposed to the air (the cool side) and the other side being exposed to the wearer's wrist (the hot side). Preferably, the device is in direct contact with the hot region. Alternatively, the device may be in contact with a thermally-conducting material which, in turn, is in direct contact with the hot region. Heat rejection from the cold side of the thermoelectric device could be to the ambient air or to any other suitably cooler medium.

The thermoelectric material may be placed in thermal contact with the first substrate. Here, "thermal contact" and "thermally attached" can encompass any connection where heat easily flows from one material to another. This does not necessarily require that the materials be in direct contact. A metallization layer (described below) may be disposed between the substrate and the thermoelectric material to ensure that these materials are in thermal contact and mechanically attached.

In power-generation devices, a "natural" temperature gradient may be used to generate power through the Seebeck effect. In these devices, the thermoelectric materials may be sandwiched between a pair of thermally conducting electrically insulating substrates.

Diamond has the highest thermal conductivity (about $2400 \text{ Wm}^{-1}\text{K}^{-1}$) of any known material. Diamond also has an extremely high degree of hardness, and is an excellent electrical insulator.

Summary

The present system describes a new kind of thermoelectric device that has advantages. Novel techniques of forming the system are also described.

An important advantage includes the ability to form a large number of thermoelectric legs due to the improved formation process.

A thermoelectric material, such as a BiTe alloy including Bi₂Te₃ and Bi₂Te₃-based alloys (in bulk or film form), may be used as the thermoelectric component. The thermoelectric material may be disposed between a first and second substrate. This material is patterned as a series of alternating μm -sized n-type and p-type regions, or "legs", on the substrates using microfabrication techniques. The area of the substrates may be larger than the area of the p and n leg region. The legs are preferably arranged in a two-dimensional "checkerboard" pattern, and at least some are electrically in series so that the output voltage is the sum of the individual voltages. The devices are thermally in parallel. Of course, the voltage potential can be controlled by connecting some of the legs in parallel as well.

The thermoelectric material is preferably microfabricated according to techniques described herein.

5 The disclosed microfabrication techniques allow forming thousands of legs, e.g., 1000-20,000 legs. They also offer the potential to achieve an appropriate voltage/current combination for a given temperature differential across a device.

10 Films of BiTe alloys deposited as legs on the substrate typically have thicknesses of between 5-100 μm . Fig. 2 shows the power output of a device as a function of leg thickness. The power output increases for a given cross-sectional area as the thermoelectric legs become thinner for a given temperature difference. This results in a higher output power density.

15 Thin films of the thermoelectric material are therefore better if the thermal resistances or electrical contact resistances are low or negligible. Thin films also allow fabrication by IC fabrication technology.

20 Electrically insulating materials having high-thermal conductivities, such as silicon carbide, aluminum nitride, boron nitride, or beryllium oxide, may be used in place of the diamond substrates. Other materials with similar electrically insulating and thermally conducting properties (i.e., as close to diamond as possible) could also be used. The desirable

25 properties of diamond and materials having similar properties enhance the effectiveness of the device. During operation, input heat from the hot side is rapidly and evenly spread out

so that the substrate efficiently supplies heat to all the n and p legs.

5 A multi-layer stack structure is preferably used to attach the thermoelectric material to the substrate. The stack structure preferably has electrically and thermally conductive materials. Electrically conductive materials provide a series electrical connection between the p- and n-doped legs of the thermoelectric material. A low electrical
10 contact resistance between the electrically conductive materials and the thermoelectric legs is desirable. This reduces the total internal electrical resistance of the device and reduces performance degradation.

Thermally-conductive materials within the stack structure
15 facilitate heat flow between the thermoelectric material and the substrate. A low thermal resistance between the heat-dissipating device and the thermoelectric material reduces heat losses. These combined factors prevent a degradation in the performance of the device. A lower stack structure having
20 a similar multi-layer configuration (and similar electrical and thermal properties) connects the thermoelectric material to the second heat-conducting substrate.

A preferred multi-layer stack structure includes a metallization layer coated on the inner surface of the
25 substrate. This thin metal coating facilitates adhesion of the substrate to other materials. In preferred embodiments, metals such as titanium or chromium are used as the substrate metallization layers. An outer diffusion barrier layer,

preferably composed of ternary alloys of metal-Si-N, where the metal is a transition metal such as Ti or Ta, may then be deposited on the metallization layer.

5 The outer diffusion barrier layer prevents the diffusion of copper to the metallization layer and to the substrate. Depending on temperature, the outer diffusion barrier may not be required. For example, at room temperature, the outer diffusion barrier may not be needed to prevent more
10 interdiffusion.

 A copper layer is deposited on the outer diffusion barrier layer. An inner diffusion barrier layer, preferably composed of Pt or metal-Si-N, is then deposited on the copper layer. The inner diffusion barrier layer impedes the
15 diffusion of copper (which has a high solid-state solubility and thus diffuses rapidly) into either the metallization layers or the thermoelectric material. Impeding the diffusion of copper prevents contamination of the other materials in the stack structure. An electrical contact layer, preferably
20 including one of the transition metals, may be deposited if required on the inner diffusion barrier layer to complete the multi-layer upper stack structure.

25 P- and n-doped thermoelectric legs of the desired thickness are deposited on the electrical contact layer. A second electrical contact layer, followed by a second inner diffusion barrier layer, is deposited on the legs.

Each layer of the stack structures is preferably deposited using semiconductor device fabrication techniques.

5 Prior processes attempted to produce sharp, patterned thick photoresist structures using microelectrical mechanical system ("MEMS") technology, which is often based on x-ray lithography.

10 The major factors which limit the power output of the device include: 1) the temperature differential across the thermoelectric legs, which is a function of the series electrical resistance of the thermoelectric legs; 2) the electrical contact resistance provided by the upper and lower multi-layer connecting structures; 3) the geometry and number of legs; and 4) the thermal resistances for heat transfer at
15 the hot and cold surfaces of the legs.

An increase in the available temperature differential will increase the available energy.

The contact resistances are particularly important with respect to thermoelectric legs of short lengths. For example,
20 the conversion efficiency of a real system is about 20% lower than the value calculated in Fig. 3 for the thermoelectric materials only. This figure shows dimensionless figure of merit which represents the performance of a thermoelectric device which depends solely upon the properties of the
25 thermoelectric material and the hot side and cold side temperatures. ZT is proportional to the square of the Seebeck coefficient divided by the product of the electrical resistivity and the thermal conductivity. The best ZT values

are obtained in heavily doped semiconductors, such as BiTe alloys, PbTe alloys and Si-Ge alloys. The electrical contact resistance arises from the connection of all the legs in series. Typical values obtained for actual generators and coolers are 10 to 25 $\mu\Omega/\text{cm}^2$. The thermal contact resistance is generated by the heat transfer characteristics of the ceramic plates and contact layers used to build the thermoelectric module. The heat exchangers and corresponding heat losses should also be taken into account.

In addition, the transport properties of the thermoelectric materials vary with temperature, as illustrated in Fig. 1. When a thermoelectric device is operating across a wide temperature range, these variations may be factored in the calculation of its performance.

The smaller size coupled with integrated circuit technology allows the devices to handle higher power densities for both cooling and generator applications. In addition, thermoelectric device miniaturization enables its operation as a power generator at much higher voltages than is possible for bulk devices, due to the much larger number of thermoelectric elements (which may be two orders of magnitude larger). These higher voltages (1 - 100 V) are more compatible with other electronic components.

While the embodiment discloses a specific use, the teachings given herein may advantageously be used in many varieties of power generation devices. The invention may

advantageously employ recovery of any kind of heat, e.g., waste heat.

5

Brief Description of the Drawings

These and other aspects of the invention will now be described with reference to the attached drawings, in which:

Fig. 1 shows a relationship between the figure of merit and temperature for various alloys;

10

Fig. 2 shows a relationship between leg thickness and specific power;

Fig. 3 shows a relationship between conversion efficiency and ZT;

15

Fig. 4 shows a prior art diagram illustrating using a thermoelectric material in a wristwatch;

Fig. 5 shows a perspective view of the assembled preferred microcooler of the preferred embodiment;

Fig. 6 shows a cross-sectional view of this preferred microcooler;

20

Fig. 7 shows a simplified electronic layout of the preferred thermoelectric device;

Fig. 8 shows a formation setup for the preferred device;

Fig. 9 shows a relationship between deposition and pH in the preferred layout;

25

Fig. 10 shows a voltammogram of the preferred materials used according to the preferred layout;

Fig. 11 shows a relationship between anodic and cathodic potentials and deposition characteristics for the preferred layout;

5 Fig. 12 shows the influence of electrolyte concentrations on stoichiometry;

Fig. 13 shows the characteristics of the electro-chemically deposited BiTe alloy;

10 Fig. 14 shows the smoothness and structure of the surface of the electro-chemically grown BiTe film;

Fig. 15 shows a relationship between the doped concentration in solution and the doped concentration which is actually applied;

15 Fig. 16 shows the relationship between the deposition voltage and what is actually deposited;

Fig. 17 shows a structure of p-type BiTe alloy;

Fig. 18 shows a graph of electrical resistivity as a function of temperature for n-type materials,

20 Figure 19 shows carrier mobility as a function of temperature;

Figs 20A - 20D show the formation of thick film photoresist deposition and patterning;

Fig. 21 shows the mushrooming effect;

25 Figs. 22A and 22B show use of electro-chemical deposition to form patterned photoresist layers;

Figs. 23A-23H show a first formation technique according to the present system;

Figs. 24 and 25 show an interdigitated technique;

Fig. 26 shows properties of the interdigitated technique;

5 Figs. 27A-27D show a simplified formation technique similar to that shown in Fig. 23.

Figs. 28A-28L show the formation sequence for the interdigitated technique.

Detailed Description

10 The preferred power-generation features a thermoelectric material in the form of a 5-100 μm thick film, operating in combination with a high-thermal conductivity, high-electrical resistivity material, preferably diamond. The system uses a thermal gradient to generate its useful power.

15 A preferred configuration shown in Fig. 4 is a cross-section of a wristwatch. A first substrate has a surface which is placed in thermal contact with a "hot" region 1003. During operation, heat flows away from the hot region and into the substrate. The heat is then incident from the substrate
20 on a first surface of the thermoelectric device 1002. A second surface of the thermoelectric material is kept cooler in operation than the first surface. This results in a voltage potential being created across points of the thermoelectric device.

25 For example, when used in a wristwatch application as in Fig. 4, the first substrate surface may be a skin-abutting surface and may be placed in contact with a user's wrist. The

second substrate surface would be exposed to the ambient air. The power from the device powers the timekeeper 1001.

5 Figs. 5 and 6 show different views of the device. The device 10 generates power using a temperature differential between a hot region 13 and a cooler region 27. Device 10 has an upper substrate 12 and a lower 12' substrate positioned over the top and bottom surfaces of a BiTe alloy-based thermoelectric element 14. The cooler region 27 is shown
10 adjacent substrate 12.

The perspective view of Fig. 5 is upside-down compared to the orientation of the device 10 in Fig. 6. The thermoelectric elements 14a, 14b are electrically in series but thermally in parallel. Each element is a "leg." A
15 thermoelectric leg is a single thermoelectric element made of n-type or p-type thermoelectric material used in fabricating a thermoelectric couple, the building block of thermoelectric modules. The geometry of the leg (cross-section to length ratio) is optimized to maximize the performance of the device.
20

The preferred thermoelectric microdevice preferably has several thousand elements compared to only about 100 to 250 in bulk devices.

25 The general requirements for substrates 12, 12' include a high thermal conductivity and a high electrical resistivity. Suitable materials include diamond, alumina, aluminum nitride, high resistivity silicon, and other such materials having similar properties. Substrates 12, 12' may be in bulk form,

e.g., about 100-1000 μm thick, e.g., 300 μm . The overall thickness of device 10 may be about 200-2000 μm , e.g., 700 μm , in some configurations. The exact dimensions are linked to the thermal environment and requirements of the device.

Thermoelectric material 14 is composed of adjacent, alternately spaced p-doped 14a and n-doped 14b legs of BiTe alloy semiconductor material. P- and n-doped legs 14a and 14b are formed by doping BiTe alloys with suitable elements as described below. Thermoelectric thick film material 14 may be about 1-100 μm thick, e.g., 50 μm . These BiTe alloy materials are preferably not bulk materials, but are deposited using microfabrication techniques, electrochemical deposition, vapor deposition, sputtering, etc. as described in considerable detail below. Each leg is separated from substrates 12, 12' by an upper 11 and a lower 11' multi-layer stack structure.

Multi-layer structures 11, 11' include metallization layers 18, 18' for metallizing a portion of the substrates' surfaces. Metallization layers 18, 18' facilitate adhesion between each substrate and subsequent layers of upper stack structures 11, 11'. Metallization layers 18, 18' also provide good mechanical connections between the substrate and a diffusion barrier. In preferred embodiments, the metallization layers include titanium, chromium, or any other electrically-conductive material which can be used to bond subsequent layers.

Outer diffusion barrier layers 20, 20' are sandwiched between metallization layers 18, 18' and copper layers 22,

22'. Outer diffusion barrier layers 20, 20' prevent diffusion of copper or other material into the substrate and metallization layers. Copper diffusion into these layers causes problems such as disruption of the mechanical bond between the substrate and the metallization layers. Outer diffusion barrier layers 20, 20' preferably include ternary alloys of metal-Si-N or any other material suitable to prevent interdiffusion of copper.

High conductivity material, e.g., copper, is used for conductive layers 22, 22' and 22a as it has a high electrical conductivity. These are used to efficiently conduct current from the p- and n-doped thermoelectric legs 14a and 14b. Copper is also an excellent thermal conductor and is used during operation to conduct heat from/to the substrates to/from the thermoelectric material.

Conductive layer 22 is connected via solder bumps 24, 24a to inner diffusion barrier layer 26. A wide range of metal alloys can be used as solder, with lead, tin, and indium alloys being preferred. Copper provides a solder-wettable surface when coated with a thin layer of nickel or palladium, and thus it may be desirable to deposit one of these materials prior to forming the solder. Generally, the solder should be placed between the Cu layer and the thermoelectric material: the specific location is variable.

The other materials are described in our previous patent No. 5,712,448, which is incorporated by reference.

The materials, thicknesses, and primary functions of each layer in the stack structures are summarized in Table I, below.

5

Table I - Layers of the Device

Layer	Ref. Numeral	Material	Thickness	Function
Heat conducting substrates	12, 12'	diamond	100-1000 μm	thermal conductor
10 Metallization layers	18, 18'	Ti, Cr	0.02 μm	adhesion
Outer diffusion barrier layers	20, 20'	metal-Si-N, Pt	0.1 μm	prevents diffusion of Cu into substrate
15 Conducting layers	22, 22'	Cu	0.1-5 μm	thermal/electrical conductor
Inner diffusion barrier layers	26, 26',	metal-Si-N, Pt	0.1 μm	prevents diffusion of Cu into thermoelectric device element
20 Electrical contact layers	28, 28'	Trans. metals	0.1 μm	electrical contact
Thermoelectric material	14, 14a, 14b	BiTe (n,p-doped) or alloys thereof	5-100 μm more preferably 20-50 μm	thermo-electric generator
25				

Preferably, there are 1000-20,000 legs, more preferably 2500-5000 legs.

30

Fig. 7 shows a simplified cross-section side view of device 10 shown as using only six thermoelectric legs. The six legs include a series of alternating p-doped 14a and n-doped 14b legs that are electrically connected in series by multi-layer upper 11 and lower 11' stack structures. Diamond layers 12, 12' provide a heat path to operate the devices in thermal parallel.

Device 10 operates based on power produced by a thermal gradient. For purposes of discussion, multi-layer upper stack structure 11 is assumed to be in contact with heat reservoir 21 that is at a lower temperature than that contacting multi-layer lower stack structure 11' (shown as element 23). Thus, a thermal gradient is established between upper stack structure 11 and lower stack structure 11'. This causes an electrical potential to be produced between the hot and cold sides of the thermoelectric generator because of the Seebeck effect. A current will pass through the legs in one direction (shown in the figure as clockwise) if the thermoelectric generator is connected to an external load, such as electronic device 38.

This voltage and subsequent current can be used to power an electronic device 38 with or without a suitable power conditioning element 21.

For example, in the case of a wristwatch, upper substrate 12 is in thermal contact with the ambient air. Lower substrate 12' is in thermal contact with the user's wrist, which is presumed to be warmer than the ambient air.

The generated current passes through a lead 40 to a first portion 11" of lower stack structure 11'. Current flows from lower stack structure 11', through first p-doped leg 14a, and into upper stack structure 11. The current then proceeds to pass through successive p-doped and n-doped legs, finally exiting through a portion 11''' of lower stack structure 11'. The current then passes through a lead 42 back to electrical device 38 to complete the circuit.

Each p- and n-doped leg of the thermoelectric material simultaneously creates a voltage from "cold" side 21, through the thermoelectric material, and to "hot side" 23.

During operation, heat first passes from the hot region to lower substrate 12'. As described above, heat is rapidly spread out and conducted due to the high thermal conductivity of the substrate. This process accumulates heat and directs the same to the thermoelectric elements. The presence of cold side 21 of the thermoelectric material results in a thermal gradient.

Fig. 2 demonstrates that the electrical power density, i.e., the electrical power per unit area generated by the device, is inversely proportional to the leg thickness for a given thermal gradient. Thus, thin thermoelectric legs (e.g., thicknesses of about 100 μm or less) result in high power densities. Details of such dependencies are described in "Thermoelectric Power Conversion," by Jean-Pierre Fleurial, incorporated by reference.

Devices operating with low ΔT heat sources can require larger numbers of legs and electrical connections for operation. The overall effect can be to substantially increase the internal electrical resistance within the device and degrade its performance. Conversely, the thermal resistance decreases as the thickness of the thermoelectric legs decreases. These effects can decrease the efficiency of the device. Use of high thermal conductivity substrates (e.g., diamond) to conduct heat into and away from the thermoelectric elements is thus important for efficient operation of small-scale devices such as consumer electronics.

The electrical and thermal properties of the multi-layer upper and lower stack structures also affect the performance of the device. The efficiency of the device decreases as the electrical contact resistance between the n- and p-doped legs containing the thermoelectric material is increased. The development of ohmic contacts to the p- and n-doped legs becomes a large factor in determining the performance as the thickness of the thermoelectric material decreases. For instance, the electrical contact resistance between a bulk thermoelectric leg and the multi-layer stack structure is typically about $10^{-5} \Omega\text{-cm}^2$ for a device having a leg thickness greater than 1 millimeter. However, for a device with a leg thickness between 5-100 μm , e.g., 10 μm , the electrical contact resistance between the stack structure and the leg must be reduced to about $10^{-6} \Omega\text{-cm}^2$ to prevent a substantial

decrease in the energy conversion efficiency and the power density of device 10.

5 The device can be used to generate power under both steady-state and transient conditions. The device generally operates at high power levels proportional to the temperature differential of the hot and cold surfaces. For applications where the temperature differential is not constant, additional power conditioning may be required. Such
10 transient conditions may be accounted for and dampened by use of the power control module 21.

In a wristwatch, the resulting output voltage V_{out} may vary somewhat throughout the typical user's day as the ambient temperature and the user's biological temperature
15 (e.g., temperature of the user's wrist) varies. Power control module 21 may be designed to account for such variations.

Power control module 21 can include a power storage element 38, e.g., a rechargeable battery or a capacitor which
20 stores the energy generated by the device at times when power output is above that needed to operate the load, such as a chronometer. Power control module 21 releases energy when power output is below that needed for operation. In many cases, power control module 21 will be an active element.
25 Power control module 21 effectively reduces power spikes in the device to improve performance.

During steady-state operation, the device may continually generate power for long periods of time.

In this case, current is continuously generated by the device under a thermal gradient to effectively power the electronic device. In this situation, a power conditioning module may
5 not be required.

Fabrication

The multi-layer stack structure shown in Figs. 5-6 is initially fabricated by depositing the conducting and
10 diffusion barrier layers on a substrate. In general, all layers are formed and patterned using fabrication techniques that are commonly used in microelectronics. For example, metals are sputtered, vacuum evaporated, or plasma deposited in reaction chambers as films. The processes for forming the
15 different layers of the stack structure (especially the metallization and copper layers) may be performed in the same reaction chamber. Likewise, the thick film thermoelectric legs are typically deposited or attached to the stack structures using a separate reaction chamber or an
20 electrochemical bath depending on the deposition technique as described below.

In a preferred fabrication method, the lower substrate is metallized to improve its adhesion to the diffusion barrier layers of the multi-layer stack structure.
25 Metallization is performed by depositing a thin metal film on a surface of the substrate. The metallization layer is followed by sequential deposition of the outer diffusion barrier, copper, inner diffusion barrier, electrical contact,,

thermoelectric material, electrical contact, diffusion barrier, and solder bump.

5 The upper substrate is sequentially coated with metallization, diffusion barrier, and copper layers. These layers are preferably patterned on the upper substrate at the same time that the lower substrate is patterned. This can be done by placing the substrates side-by-side in the appropriate reaction chambers. As described above,
10 deposition is preferably performed using plasma or sputter deposition or vacuum evaporation. The desired pattern of each film is then obtained using spatially filtering masks, photolithography, and etchants commonly used in microelectronics fabrication.

15

DIFFUSION BARRIERS

The fabrication of thick film thermoelectric microdevices is based on the deposition of films in the 10-100 micron thickness range as well as the prevention of
20 degradation of the thermoelectric material upon post-deposition heat treatments of the thermoelectric elements or operation of the completed device at elevated temperatures. The commonly-used diffusion barrier materials do not prevent the diffusion of Cu into the thermoelectric elements.

25 A preferred diffusion barrier prevents performance degradation of thermoelectric devices due to Cu or solder migration into the thermoelectric elements. Tests performed to measure such diffusion have shown no migration through the

inventive barriers at 350°C for 1 hour. By comparison, commonly used barrier materials such as Ni, Pt, and Pd indicated Cu diffusion at 200°C after 1 hour. The formation of diffusion barriers is described in "Films of Ni-7%V,...", J. Appl Phys, 31 (1998). This describes that high electrical conductivity materials such as aluminum and copper are commonly used as the interconnection material in IC, silicon based, and in thermoelectric, BiTe based, devices. However, diffusion of these high conductivity materials into the silicon or BiTe can result in a reduction of performance so it is frequently necessary to provide a barrier to prevent in diffusion. Metal films of Ni-7 at% V, Pt and Pd were shown to fail to prevent interdiffusion of Cu and BiTe after a few hours at 200°C. However, the Ta₄₀Si₁₄N₄₆ barrier preserves the integrity of the contact after anneals of 200°C for 50 hours and 350°C for 1 hour.

A summary of the parameters of the sputtered films is shown in Table II.

Table II

-Cleaning:

Acetone and Isopropanol (both ea. 30"), dry blow

-Sputtering

Base pressure: -5.10^{-7} mbar

Material	Target	Thickness	Gas flow	Total gas pressure
TaSi	TaSi	50 nm	Ar, 60sccm	4 mbar
Cu	Cu	1 μ m	Ar, 60sccm	10 mbar
TaSiN	TaSi	100 nm	Ar, 60sccm/N 2sccm	4 mbar
Pt	Pt	0.5 μ m	Ar, 23sccm	5 mbar

A solder bump 24 may be electroplated on a region of each diffusion barrier 26. The upper and lower substrates are stacked on top of each other and aligned. The substrates are then heated to a temperature which melts solder bump 24 and solders the copper layer of the upper substrate to the exposed inner diffusion barrier layer of the lower substrate. Conventional soldering or brazing is not the preferred method for attaching the copper and diffusion barrier layers due to the small size of the doped legs. Solder bump 24 collapses and fuses the copper layer 22 and the diffusion barrier 26 layer on heating to its melting temperature. Surface tension of the molten solder prevents bridging between the neighboring doped legs of the thermoelectric material, thereby reducing the probability of electrical shorting during operation.

The electro-chemical deposition (ECD) method for thermoelectric element growth has a significant advantage for device fabrication. Since the thermoelectric elements can be grown on a substrate, the substrate can be coated with a mask to cause the elements to grow on an interconnect bus pattern already on the substrate. By doing this, conventional IC fabrication technologies can be adapted to the production on micro thermoelectric devices for volume production. Thermoelectric films may also be deposited on the stack structures using other well-known techniques such as molecular beam epitaxy, CVD, sputtering, evaporation.

Heat treating, as described above in connection with ECD-grown films, is particularly important for films deposited by sputtering or flash evaporation. Heat treatment improves crystallinity in grain size. Heat treatment also anneals carrier generating defects, such as tellurium vacancies, or anti-structure defects, and other defects.

The patterns of the thermoelectric legs are isolated to assure that current flow only occurs through the doped legs. Preferably, a "checkerboard" pattern is formed. Typical spacing between the legs is between 5 and 100 μm . A typical cross section of both the n- and p-doped legs within this pattern is 10x10 to 100x100 μm .

One way of depositing the thermoelectric device legs is by electrodeposition. These legs have typical dimensions of much less than a millimeter. In particular, the thermoelectric device legs may have sizes of a few μms to a few tens-of- μm in width and/or length.

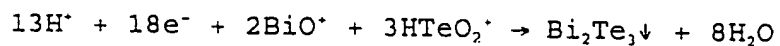
In a typical fabrication process, once contact layer 28' is deposited as described above, the structure is placed in an electrodeposition bath and forms the cathode (or working electrode). Electro-chemical deposition is performed as described below. Photoresist is previously applied to define the area to be patterned. Patterns are etched onto the photoresist layer using photolithography where legs are desired. A shallow Pt layer may be deposited on the structure prior to the structure entering the bath to protect the already-deposited layers.

ECD is effectively used to deposit thick BiTe alloy films. Electro-chemical deposition has been extensively used for CdSe, CdTe, and alloys, achieves a high deposition rate on metallic substrates, and may be performed at room temperature. Thus, electro-chemical deposition is inexpensive and scalable.

ECD OF N-TYPE BiTe ALLOY THICK FILMS

For electrodeposition of n-type legs, the bath typically includes Bi, Te, Sb, and Se. With reference to a standard calomel electrode, voltages of about -5 mV up to about -60 mV can be used to deposit n-type BiTe alloys, e.g., Bi_2Te_3 or $\text{Bi}_2\text{Te}_{3-x}\text{Se}_x$ or $\text{Bi}_{x-2}\text{Sb}_x\text{Te}_{3-y}\text{Se}_y$.

In particular, bismuth and tellurium metals dissolve in nitric acid (HNO_3) to make the oxide anions BiO^+ and HteO_2^- . The binary compound BiTe alloy is insoluble in dilute HNO_3 , so the reduction of the anions to Bi^{3+} and Te^{2+} at an electrode surface will result in the precipitation of BiTe alloys on the surface. The overall reaction for the process is:



To realize the production of stoichiometric BiTe alloy thick films with the desired thermoelectric properties, the process parameters must be optimized. These parameters include: electrolyte pH; molar concentrations of the Bi and thermoelectric in the HNO_3 solution; Bi and thermoelectric

feedstock materials; temperature; electrolyte stirring;
substrate surface finish; electrode geometry; voltage; and
current density. By introducing suitable amounts of Se into
5 the electrolyte, optimum $\text{Bi}_2\text{Te}_{1-x}\text{Se}_x$ alloy compositions
($0.15 < x < 0.6$) can be prepared by the same technique.

Electro-chemical deposition of Bi, Te and Se from
aqueous solutions of nitric acid may be performed as
described below to form materials with good thermoelectric
10 properties. Electro-chemical deposition tests have been
performed to validate the growth of $\text{Bi}_2\text{Te}_{1-x}\text{Se}_x$ n-type
thermoelectric elements with satisfactory thermoelectric
performance. Because of the multiplicity of parameters
possible, the preferred configuration for the electro-
15 chemical deposition process, and its rationale, is discussed
below.

Setup

A typical configuration for producing such n-type thick
20 films is illustrated in Fig. 8. The main elements of the
setup include: electrolyte 102 in a glass container; cathode
electrode which forms the substrate for n- or p-type
thermoelectric element growth; platinum anode electrode 106,
also referred to as the "counter electrode"; reference
25 electrode 108; and stirrers as needed, and a power supply
system 110 to provide a constant monitored voltage or current
during deposition. The electro-chemical deposition can be

performed in an open beaker while using normal laboratory precautions when working with low pH acid-aqueous solutions.

5 Electrolyte

Bi, Sb, Te, and Se are soluble in acids (both the metals and their compounds) so the electrolyte can be an acid solution. Common acids such as hydrochloric (HCl) and sulfuric (H₂SO₄) acids may be used for the electrolyte so long
10 as they do not dissolve other materials to be used in the device fabrication. An aqueous solution of nitric acid (HNO₃) may be preferable for the electrolyte.

Electrolyte pH

15 The electrolyte pH will have an important effect upon the electro-chemical deposition process since it will determine the concentration of the Bi, Sb, Te, and Se ions in solution. The concentrations of these ions in turn influence the rate of deposition and thus the rate of film growth.
20 High quality films can be grown in a 1 molar aqueous solution of nitric acid, which corresponds to a pH of 0. pH levels of -1 to +1 may also be used. At this pH, Bi, Te, and Se dissolve to concentrations useful for electro-chemical deposition while the electrodeposited BiTe alloy is not
25 dissolved. Additionally, this pH value is compatible with the other materials (metallizations, photoresist, substrates, etc.) that operate in the electrolyte. A zero pH enables a high solubility of tellurium in the one molar nitric acid

solution. In particular, at a zero pH, the Te concentration equals 10mM which is very close to the solubility limit.

5 Electrolyte Temperature

Room temperature (18°C) operation produces very uniform BiTe alloy films that display good thermoelectric properties. Elevated or reduced temperatures do not appear to offer any advantages.

10

Electrolyte Agitation (Stirring)

The electro-chemical deposition process is most likely diffusion-limited. That is, the region of the electrolyte in the immediate proximity of the film is constantly being
15 depleted of the anions in solution. As such, it may be important to agitate or stir the solution so that the anion population is replenished. If there were no agitation, the source of anions would be "diffusion" limited. Tests demonstrated that a simple magnetic stirrer was sufficient to
20 provide bulk movement of the electrolyte.

The setup can also be run in an inert atmosphere such as Ar by purging the electro-chemical deposition cell from oxygen with bubbling Ar into the electrolyte. In some cases this can lead to improved film morphology since there is no
25 generation of hydrogen peroxide gas at the working electrode.

Working Electrode/Photoresist

Working electrode is the substrate with interconnect bus and photoresist which defines where the n-type material is deposited.

The substrate is an essential component of the integrated microcooler/microgenerator devices. The substrate will serve the purpose of conducting the heat into and out of the active components (i.e., the n-type and the p-type elements) of the devices. The substrate will also have the interconnect electrical bus deposited onto it so that the n- and p-type elements can be grown in the proper location so as to create a complete electrical circuit.

The interconnect bus work may be attached to the substrate as a thin film in a pattern suitable for depositing the n-type elements at the desired location. This patterning is made possible by coating the substrate with a thick photoresist, preferably of a thickness at least the same as the desired height of the thermoelectric element. The photoresist may then have holes etched into it in the pattern corresponding to the location of the n-type thermoelectric elements. The pattern in the photoresist would then correspond to the pattern of the interconnect bus on the substrate.

The interconnect bus should have low chemical resistance. Copper is a good material. However, copper can diffuse into BiTe alloy which in turn degrades thermoelectric performance. Thus, the bus is preferably coated with the

diffusion barrier layer prior to copper coating. The final coating on top of this diffusion barrier layer has to be compatible with the aqueous acid solution. A suitable material is platinum (Pt) and so this is the preferred material onto which the BiTe alloy is electrodeposited. A contact layer such as Bi can also be deposited on top of the Pt coating prior to BiTe alloy deposition in order to improve mechanical bonding after suitable heat treatments. To assure uniform growth and a smooth texture to the electro-chemical deposition elements, the substrate may have a smooth surface. The substrate is connected to the negative terminal of the deposition power supply.

15 Counter-Electrode

The counter electrode 106 completes the circuit in the electro-chemical deposition electrolyte. Since 106 is the positive, or anode, electrode, nothing is deposited on it. Thus, the counter electrode is preferably compatible with the aqueous acid solution and for this purpose, platinum may be used.

20 Reference Electrode

The reference electrode 108 should provide a stable measure of the deposition potential so that the power supply can be operated at the desired voltage. This is particularly important since the voltage can influence the composition and uniformity of the deposited film. A calomel (Hg/HgCl)

electrode was used since it is compatible with the electrolyte and the electro-chemical deposition operating conditions. Since there is the possibility of a slow leakage
5 of Cl from the calomel electrode, it is placed in a second container and filled with a KNO_3 solution. A capillary bridge filled with glass wool and KNO_3 was used to make the complete electrical connection to the electro-deposition solution.

A no-leak reference electrode (such as Ag/AgCl) can also
10 be used directly into the electrolyte solution, thus eliminating the need for a salt bridge and a separate beaker.

Bi Feedstock and Concentration

Bismuth, in the elemental metallic form, is soluble in
15 an aqueous solution of HNO_3 . For this reason, it was the preferred source of Bi in the electrolyte. Bi could, of course, have been supplied in other compound forms. However, there may be concern about interference from other elements introduced into the electrolyte. The concentration of
20 dissolved Bi, [Bi], is an important parameter that may be coordinated with the concentration of Te, [Te], (or [Te+Se]) to assure the growth of films with the preferred [Te]/[Bi] ratio (or [Te+Se]/[Bi+Sb] ratio). This ratio will have an effect upon the thermoelectric performance of the deposited
25 films. The actual mole ratios in solution are discussed below. Because of the low pH of the electrolyte, Bi could be dissolved to concentration in the range of 0.5 to $10 \times 10^{-3}\text{M}$. However, for high quality n-type thermoelectric thick films,

with acceptable growth rates, concentrations in the range of 5 to $10 \times 10^{-3} \text{M}$ may be the most productive.

5 Sb Feedstock and Concentration

 The preferred feedstock for the antimony was the elemental form, although Sb_2O_3 could also be used without introducing additional elements into the electrolyte. Sb salts are also suitable but they typically introduce
10 contaminants such as Cl or F. Figure 9 shows the solubility of the different materials. Compared to Bi or Te, Sb has a more limited solubility, up to $9 \times 10^{-4} \text{M/l}$, in the 1 molar nitric acid solution, so Sb was the determining constituent for the Bi and thermoelectric concentrations.

15 Without any chelating agent, and to obtain stoichiometric BiTe alloy films, typical Sb concentrations used for electro-chemical deposition were in the range of 0.1 to $0.9 \times 10^{-3} \text{M}$. Using these concentrations, the complete range of BiTe alloy solid solutions could be obtained, as
20 shown in Fig. 15. However, due to the low concentrations of the elements in the electrolyte, typical deposition rates for the film were on the order of $1 \mu\text{m/hour}$ (typical current densities were less than 0.6 mA/cm^2). To increase the deposition rate, higher Sb concentrations were prepared by
25 introducing chelating agents such as tartaric acid ($\text{C}_4\text{H}_6\text{O}_6$) EDTA and EGTA. Using tartaric acid (a very weak acid that does not change the overall solution pH), [Sb] concentrations up to $8 \times 10^{-2} \text{M}$ can be prepared (two orders of magnitude higher

than without tartaric acid) and are stable at room temperature. E.g., for a calculated [Sb] solubility of [Sb] = 0.85 mM, the achieved [Sb] was 0.7 mM at pH = 0.

5 Experiments show that films deposited at high electrochemical deposition voltages and low antimony concentrations result in films having a rough, sponge-like surface. In addition, these films are thin due to the low deposition rate (1-2 μm per hour). In contrast, films deposited at a lower
10 voltage but at higher antimony concentrations were considerably smoother, and could be grown more rapidly (e.g., 10 μm per hour).

Te Feedstock and Concentration

15 As with Bi, the elemental form of thermoelectric is soluble in 1 molar aqueous nitric acid. This may be the preferred form of feedstock since other elements would not be introduced into the solution. Te is also soluble in the range of 0.5 to $10 \times 10^{-3}\text{M}$. To facilitate rapid film growth,
20 the concentration of greatest interest was in the range of 5 to $10 \times 10^{-3}\text{M}$.

Se Feedstock and Concentration

The elemental form of Se is soluble in 1 molar aqueous
25 nitric acid. Se is also soluble in the range of 0.5 to $10 \times 10^{-3}\text{M}$. To facilitate rapid film growth and to achieve the desired BiTe alloy composition ($0.15 < x < 0.45$), the

concentrations of greatest interest were in the range of 0.5 to $2.5 \times 10^{-3} \text{M}$.

5 [Te]/[Bi] Mole Ratio in Solution

One objective was stoichiometric BiTe alloy films for their optimized thermoelectric performance. Other parameters affect the uniformity and composition of the electro-chemical deposition films, but certainly the mole ratio has a significant effect. For depositing BiTe alloys, [Te]/[Bi] mole ratios of 1 to 2 were evaluated (i.e., the [Bi]/[Te] ratio was determined to be in the range of 0.7 - 0.8 following tests where the ratio was varied from 0.1 to 3.5). Typical concentrations that produced acceptable films were $10 \times 10^{-3} \text{M}$ of Te and $8 \times 10^{-3} \text{M}$ of Bi ([Te]/[Bi]=1.25). For depositing BiTe alloy compositions (with $0.15 < x < 0.45$), it was determined that similar anion to cation mole ratios could be used ([Te+Se]/[Bi]=1.1 to 1.5) by adding small amounts of Se to the electrolyte. [Te]/[Se] mole ratio values of 5 to 10 were used to achieve the desired ternary compositions.

These ratios were found to be appropriate if concentrations are kept fairly high, greater than about 4mM. The results are significantly different if using low-element concentrations, such as around 1mM.

25 N-type $\text{Bi}_{1-x}\text{Sb}_x\text{Te}_3$ films were also prepared by using a suitable electrolyte composition [Bi]-0.4[Sb]-1.6 [Te]-0.7 and 2mM $\text{C}_4\text{H}_6\text{O}_6$ and voltage ~60mV.

ECD Voltage and Current Density

Voltammograms were measured for the reduction of both BiO^+ and HTeO_2^+ on platinum substrates. Fig. 10 shows a
5 voltammogram of Bi and Te deposited on platinum. A 7mM concentration of Bi is provided, along with a 10mM concentration of Te in 1M nitric acid. Working and counterelectrodes of platinum are used.

Both Bi and Te were observed to deposit at voltages in
10 the range of 0.0 to -0.2V versus a standard Hg/HgCl calomel electrode. A co-deposition voltammogram for a Bi/Te electrolyte is shown in Fig. 11. Thus, co-deposition of Bi_2Te_3 in a range of voltages from 0 to -0.1V may be performed. Development of the electro-chemical deposition
15 process has shown that a voltage in the -2 to -10mV range, versus a standard Hg/HgCl calomel electrode, produces the desired BiTe alloy films. At these voltages, typical current densities are in the range of up to 8 mA/cm² and produced film growth rates in the range of 1 to 15 $\mu\text{m/hr}$. Higher voltages
20 may be used, e.g., -60 mV, but higher voltages also tend to produce dendritic growth. The micrographs in Figs. 20A - 20D show 30 μm thick BiTe alloy columns grown within columnar holes initially etched into a thick photoresist layer. Figure 12 shows the influence of the concentrations of
25 electrolytes on the final film. Fig. 13 shows the x-ray diffraction pattern of a BiTe alloy film, as-deposited and after a short heat treatment.

In addition to the deposition voltage, the growth rate is also controlled by electrolyte stirring, element concentrations, and temperature. Similar deposition voltages were used for depositing $\text{Bi}_2\text{Te}_{3-x}\text{Se}_x$ compositions (with $0.15 < x < 0.45$).

Fig. 14 shows a micrograph of ECD-grown BiTe alloy films. Such films may be deposited on a variety of substrates, such as Mo, platinum, stainless steel, metallized silicon, metallized aluminum nitride, and metallized diamond. As may be seen, the top surfaces of such BiTe alloy films are relatively smooth. Their roughness may be less than one micron. Generally, their smoothness depends on substrate texture, roughness, and growth rate.

N-type Performance

Measurements of the electrical transport properties have been conducted on some of the as-deposited films. Van der Pauw electrical resistivity and Hall effect (coefficient and mobility) are measured in the plane of the deposited films (after removal by delamination from the metallized electrically conducting substrates (for these measurements, the films should be at least $30\text{ }\mu\text{m}$ thick)), and the Seebeck coefficient was measured in a cross-plane direction. For the latter measurement, a small ΔT was applied across the film thickness. In addition, the sample may be left on the electrically conducting substrate (e.g., the Pt substrate) and thermocoupled pressure contacts may be

applied. In addition, thermal conductivity measurements may be made using the 3 ω technique. The transport property measurements were primarily made at room temperature although
5 some samples were measured in the 80-400K range.

Results show heavily doped n-type behavior with high electron concentrations ($\sim 1 \times 10^{20} \text{cm}^{-3}$) and relatively low Hall mobility values ($\sim 15\text{-}25 \text{cm}^2/\text{Vs}$). Resistivity values (parallel to the C axis) were measured to be $\rho = 12 \text{m}\Omega \cdot \text{cm}$. These results
10 were true regardless of the deposition voltage provided that [Bi] and [Te] concentrations were several mM (e.g., greater than 4). Seebeck coefficient values ranged from $-50 \mu\text{V/K}$ to over $-100 \mu\text{V/K}$ near room temperature.

$\text{Bi}_2\text{Te}_{2.9}\text{Se}_{0.1}$ alloy films show n-type behavior, although
15 not heavily doped.

Annealing

Post-ECD heat treatments improve the thermoelectric performance of the as-deposited thick films. Systematic
20 experiments have shown that heat-treatments in the range of 150 to 300°C for 1 to 250 hours in an inert atmosphere (or vacuum or hydrogen) promotes annealing of crystal defects responsible for the high electron concentrations and poor carrier mobilities. This is illustrated in Figs. 18 and 19
25 by the sharp increase in carrier mobility (Fig. 19) and corresponding decrease in electrical resistivity (Fig. 18) for a Bi_2Te_3 film.

Carrier concentration (i.e., doping level) is usually controlled by stoichiometric deviations. The electrical properties are improved by anneals. For example, doping levels decrease when carrier mobilities increase. The Seebeck coefficient increased to $-200 \mu\text{V/K}$ after a 250°C anneal. In addition, Hall mobility increased to about $80 \text{ cm}^2/\text{Vs}$. Typical heat treatment conditions in a vacuum environment leading to good thermoelectric properties are $200\text{-}300^\circ\text{C}$ for a few hours or longer, e.g., 250°C for a 48-hour period. Heat treatments may occur in vacuum, hydrogen atmospheres, or inert atmospheres such as argon.

Since heat treatments are an integral part of the thermoelectric element fabrication process, the role of a stable diffusion barrier is important to prevent rapid degradation from Cu and/or solder contamination of the thermoelectric material.

It is also noted that Sb could be used to increase the Seebeck coefficient and to enhance electrical conductivity; however, too much Sb will cause the deposited film to switch to p-type.

The above describes the growth of the n-type legs. The p-type legs are formed using a similar operation.

ECD OF P-TYPE BiTeSb THICK FILMS

ECD of Bi, Sb, and Te from aqueous solutions of nitric acid is useful and thick films with good thermoelectric properties can be made reliably. Electro-chemical deposition

tests have been performed to validate the growth of BiTe alloy p-type thermoelectric elements with satisfactory thermoelectric performance.

5

Setup

A typical configuration for producing p-type thick films is the same as shown in Fig. 8. The main elements of the setup are an electrolyte in a glass container 102; a cathode electrode 104 (the substrate for thermoelectric element growth); a platinum anode electrode 106 (also referred to as the "counter electrode"); a reference electrode 108; a stirring rod (not shown); and a power supply 110 to provide a constant voltage during deposition. The electro-chemical deposition can be performed in an open beaker while using normal laboratory precautions when working with low pH acid-aqueous solution.

The electrolyte is also the same as described above for n-type, as is the electrolyte pH, Electrolyte Agitation (Stirring), Substrate Interconnect Bus/Photoresist, Counter Electrode, and the Reference Electrode.

Bi Feedstock and Concentration.

Because of the low pH of the electrolyte, Bi could be dissolved to concentration in the range of 0.5 to $10 \times 10^{-3} \text{M}$. This offers a broad range of concentrations. However, for the deposition of high quality p-type Sb_2Te_3 -rich $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_3$,

thick films with acceptable growth rates, concentrations in the range of 0.5 to 2.0×10^{-3} M may be the most preferred.

5 Te Feedstock and Concentration

As with Bi, the elemental form of thermoelectric is soluble in 1 molar aqueous nitric acid. This was the preferred form of feedstock since other elements would not be introduced into the solution. Thermoelectric is also soluble
10 in the range of 0.5 to 10×10^{-3} M. To facilitate rapid film growth of proper stoichiometry, the concentration of greatest interest was in the range of 1 to 8×10^{-3} M.

15 Se Feedstock and Concentration

The elemental form of Se is soluble in 1 molar aqueous nitric acid. Se is also soluble in the range of 0.5 to 10×10^{-3} M. To facilitate rapid film growth and to achieve the desired BiTe alloy composition ($0.15 < y < 0.45$), the concentrations of greatest interest were in the range of 0.5
20 to 2.5×10^{-3} M.

25 ECD Voltage and Current Density

Bi, Sb, and Te were observed to deposit at voltages in the range of -25 to -200mV versus a standard Hg/HgCl calomel electrode (see the voltammogram of Fig. 10). Thus BiTe alloys may be deposited in a range of voltages from 0 to -0.3 V, e.g., -70 mV to -150 mV. In fact, little or no deposition occurs for voltages less than about -0.08 V.

Voltammograms were measured for the reduction of BiO^+ , SbO^+ and HTeO_2^+ on platinum substrates. Electro-chemical deposition with Sb present and no chelating agent required a more negative voltage than was needed for the preparation of n-type films. Voltages ranging from -100mV to -250mV were found to produce p-type films with the required Sb_2Te_3 -rich stoichiometry e.g., 60 at.% Te). At these voltages, typical current densities were about 1 mA/cm² and produced film growth rates of about 1 $\mu\text{m/hr}$. In some situations, the surface morphology was rough and had dendrites.

To work at lower voltages (-25 to -100 mV) and higher deposition rates (5-10 $\mu\text{m/hour}$), much higher [Sb] concentrations are required to maintain the Sb_2Te_3 -rich ternary alloy composition. Typical electrolyte concentrations of Bi:Sb:Te are 1.0:32.0:4.0 (in 10^{-3}M) for such deposition experiments. At those voltages, typical current densities are in the range of up to 6-8 mA/cm² and produced film growth rates in the range of 5 to 10 $\mu\text{m/hr}$.

The micrograph in Fig. 17 shows 20 μm thick $\text{Bi}_{12}\text{Sb}_{28}\text{Te}_{60}$ film grown by this technique.

Te to Bi+Sb Mole Ratio in Solution

One objective is to produce thick $\text{Bi}_{1-x}\text{Sb}_x\text{Te}$, films with an atomic ratio similar to optimized bulk grown crystals. This means films of 75 to 90% Sb_2Te_3 , and 10 to 20% BiTe alloys. Other parameters affect the uniformity and composition of the electro-chemical deposition films, but

the mole ratio in solution has a significant effect. P-type $\text{Bi}_{0.4}\text{Sb}_{1.6}\text{Te}_1$ thick films were produced with solution concentrations of Bi:Sb:Te of 0.18:0.90:1.70 (in 10^{-3}M) without chelating agent, or 0.2:1.6:0.7 or 1:8:2 with chelating agent.

Fig. 15 shows the atomic Sb/Bi ratio in the deposited BiTe alloy film as a function of the aqueous concentrations of these elements in the electrolyte. Deposition voltage, temperature and Te concentration were identical throughout these experiments. Compositions corresponding to premium bulk alloys were obtained for $[\text{Sb}]/[\text{Bi}] - 4.5$.

As shown in Fig. 15, by keeping a constant $[\text{Sb}]/[\text{Bi}]$ ratio as well as a constant $[\text{Te}]/[\text{Bi}+\text{Sb}]$ ratio, suitable films were produced with concentrations ranging from 0.3 to $0.9 \times 10^{-3}\text{M}$ provided that the deposition voltage was maintained in a -100 to -200mV range (relatively to a standard calomel electrode). When working at lower voltages and higher deposition rates, much higher [Sb] concentrations are required to maintain the Sb_2Te_3 -rich ternary alloy composition. Suitable electrolyte concentrations of Bi:Sb:Te are 1.0:32.0:4.0 or 0.2:1.6:0.7 (in 10^{-3}M). This is shown in Fig. 16 using a 10 M concentration of BiTeSb . The introduction of suitable amounts of Se into the electrodeposited film to form quaternary solid solutions can be done by using $[\text{Te}]/[\text{Se}]$ mole ratio values of 5 to 10.

p-type Characterization of Films

The transport properties of the ternary films have been measured. Some of these films were those deposited on platinum substrates. The measurements confirmed the ternary film's p-type conductivity. In addition, the Seebeck values were shown to be sensitive to the film's stoichiometry.

Measurements of the Seebeck coefficient have been conducted on some of the deposited films. Seebeck coefficient values (measured in a cross-plane direction) as high as $250 \mu\text{VK}^{-1}$ were obtained, depending on the actual composition of the films. The electrical resistivity and thermal conductivity of these films is likely close to that of bulk state-of-the-art thermoelectric BiTe alloys.

15 Anneal

Suitable heat treatments, up to 300°C for several hours, may also be used to anneal structural defects introduced during film growth. "High" values of thermal conductivity, as used herein, refers to a level of thermal conductivity sufficient to not pose a significant thermal impedance. This may improve transport properties as in the case of n-type BiTe alloy films grown by electro-chemical deposition. For example, an anneal of 300°C for 1 hour increased the Seebeck value of one film from 57 to $93 \mu\text{V/K}$.

25 Since heat treatments are an integral part of the thermoelectric element fabrication process, the role of a stable diffusion barrier is important to prevent rapid

degradation from Cu and/or solder contamination of the thermoelectric material.

5 In all of these processes, a thick photoresist may be used to maintain the geometry of the legs. Figs. 20A - 20D show micrographs of legs grown by the above process of thick photoresist deposition and patterning.

10 In other embodiments, the hot-wall method may be used to generate the BiTe alloy-based film. This technique is used to deposit films having thicknesses as high as about 30 μm . Here, the material to be evaporated is placed in a quartz tube located inside a vacuum chamber. A substrate and solid BiTe alloy-based material are placed, respectively, in the top and bottom portions of the tube. The substrate, tube
15 walls, and BiTe alloy-based material are then heated to a temperature which causes the thermoelectric material to evaporate and form on the surface of the substrate. Individual n- and p-doped materials are formed by feeding the appropriate doped material in bulk form in the chamber.

20 Other thick film growth techniques might include those commonly used in the semiconductor fabrication industry: vacuum evaporation, CVD (chemical vapor deposition) and sputter deposition. While these techniques will probably produce thermoelectric materials with the desired
25 performance, they are best suited to devices with dimensions smaller than a micrometer due to their slower growths (when compared with ECD).

Once appropriate electro-chemical depositions of n-type and p-type thermoelectric legs are determined, the next step is to pattern the legs. For these purposes, thick
5 photoresists were developed. For example, in the prior art, photoresists are available but are rated for at most 10 to 20 micrometer thicknesses. X-ray lithography techniques allow thicker growths but are cumbersome and expensive. In the present system, very thick photoresist layers are required,
10 e.g., up to about 60 μm .

Two types of masks were developed. For the first mask, 10 square shaped patterns were provided. These squares had sizes of 50, 75, and 100 micrometers. A 200 micrometer pitch was provided. After exposing the photoresist, the squares
15 were rounded at the angles. Due to the thickness, these squares were obtained with two successive coatings. Process parameters were optimized to improve the adhesion of the photoresist and the verticality of the wall.

For the second mask, square and circle patterns were
20 provided in sizes of 10, 20, 50, and 100 micrometers. Single and double pitches were provided.

In experiments using the first mask, one aspect noted was that air trapped inside the holes required removal so that the holes could be properly wetted.

25 Initial experiments partially cracked and lifted the photoresist. This resulted in muffin-like deposits and star-like legs, as shown in Fig. 21. A solution to this was to

begin the process with a few seconds, or up to 1 to 2 minutes, of ultrasonic agitation in deionized water.

Square legs were also deposited which were 30 micrometers tall and 60 micrometers wide. Experiments showed that the leg growth mushrooms on top of the photoresist layer as soon as the leg becomes taller than the patterned hole. One remedy is to monitor the current intensity as a function of time. Once the leg becomes taller than the hole, the surface area may significantly change, significantly altering the current. By determining when the current intensity changes significantly, the time for deposition may be predetermined. Using this predetermined time, leg deposition can easily be confined to the patterned hole. Using such techniques, the successful growth seen in Figs. 22A and 22B may be obtained. Figure 22B shows depositing 11,000 legs in a 3x3 square mm area using this technique.

These legs are preferably columnar, since columnar legs may have more strength per unit size.

Leg growth may also be monitored and assisted by reversing the polarity of the electro-chemical deposition voltage once the leg height is at or above the desired height. In this way, a partial removal of materials may be effected which can make the tops of the legs more flat or which can remove mushroom growth. The mechanism for the removal is that the irregularities are preferentially removed as they cause higher electric fields to be produced in their vicinity.

Using the second mask, ultrasonic agitation in deionized water was again performed. This was somewhat more difficult to optimize due to very different pattern sizes. Legs were deposited in both square and round shapes. Characteristic dimensions included a height of 45 micrometers and a width of 20 micrometers. Very small spaces were successfully filled by electro-chemical deposition. The leg pattern was tightly conformed to the pattern geometry. The legs were confinable to the patterned hole. However, due to the increased pattern sizes after etching, only double pitch patterns in the "10 micrometer" mask could be successfully used (overlapping occurred in single-pitch "10-micrometer" patterns).

An example of the photoresist technique is shown in Table III.

Table III

Photolithography:

Resist: Shipley Microdeposit SJR5740

Coatings:

	Coating 1	Coating 2
AZ Adhesion promoter	30"	-
Dry spin	1000 rpm/20"	-
Resist dispense	Syringe (0 rpm)	Syringe (0 rpm)
Spinning	1000 rpm/10"	2000 rpm / 30"
Wait time	5'	5'
Ramp	200 °C/h (RT-105 °C)	-
Soft bake	5'/105°C	5'/105°C
Thickness	24 μm	18 μm

Exposure: 130"/-8Wcm²/405 nm

Develop: 6-10°/Clariant AZ 421K (1:1)

Figs. 23A-H show an embodiment of the fabrication method. A substrate 1202 is shown with a metallization layer 1204. A photoresist 1206 is shown in several blocks. Photoresist 1206 is initially laid down in known manner and is patterned and etched to leave interstices where the n-type legs are to be deposited. As seen in Fig. 23A, this figure shows the n-type legs already having been deposited. Referring to Fig. 23B, the photoresist layer is masked with additional

photoresist 1208 to cover the n-type legs 1210. The photomask is shifted using an aligner and is patterned in such a way as to allow etching at interstices where p-type legs are to be deposited by electro-chemical deposition. Following this shifting and etching, p-type legs are deposited in the manner described above. These p-type legs are referred to as elements 1212 in Fig. 23B. Thus, two exposures of the same photoresist are performed. In such procedures, it is difficult to perform the second step as the photoresist has already been hardened once. It may be preferable to use yellow light as the illuminating light in the first exposure step to prohibit complete hardening of the photoresist.

Fig. 23C shows all of the photoresist dissolved, leaving substrate 1202, metallization layer 1204, n-legs 1210, and p-legs 1212. Referring to Fig. 23D, an underfill material 1214 is provided between the legs. The underfill material was originally developed for flip chip technology. The underfill material 1214 generally requires curing (such as at least about 150°C for 30 minutes). The underfill material 1214 allows for further processing without loss of mechanical integrity. For example, chemical-mechanical polishing may be required and may be provided with the strengthened legs.

Referring to Fig. 23E, a diffusion barrier is then deposited on top of the legs and underfill material. At this point, electrode material 1216 may be deposited to

connect the n-type material with the p-type material in appropriate locations. The electrode material may be made of gold, tin, or other similarly conductive materials. The photomask is used to allow deposition of electrodes 1216 in desired locations. This photomask is shown in Fig. 23E as mask 1218.

Referring to Fig. 23F, a substrate 1202' is shown with similar electrode layers 1216' as are located in Fig. 23E. Substrate 1202' may be bonded to substrate 1202 and its accompanying leg structure by disposing electrodes 1216 opposite electrodes 1216'. Bonding may be accomplished using a bonder-aligner with a brief heat treatment. The precision of bonding should be on the order of 5 micrometers. The heat treatment could be for, e.g., three minutes to 300°C, and 7 minutes down to 100°C.

Referring to Fig. 23G, the growth substrate 1202 may then be removed. A new photomask may be applied and electrodes 1216" may be applied on the lower surface of the leg structure. A substrate 1202", similar in structure to substrate 1202', may then be attached to the bottom side of the leg structure by disposing electrodes 1216" opposite electrodes 1216". In this manner, the appropriate electrical connections may be made for all of the thermoelectric legs.

The structure may be used as shown in Fig. 23G, in which the underfill is retained in order to allow a very

high ruggedness for the device. Alternatively, for appropriate applications, the underfill material may be removed, as shown in Fig. 23H.

5 Figs. 24-26 show another embodiment of a growth method, termed a "bipotentistat" method. Using this technique, legs of both doping types may be grown without the need to cover legs of one type with a cover layer as is necessary in the embodiment of Figs. 23A-
10 23H.

Fig. 24 shows two working electrodes 3902 and 3904 are disposed in a first bath 3901, which may be NHO_3 . The substrate may be placed on one of the working electrodes as dictated by the requirements of the
15 process. A mesh counter-electrode 3906 is also disposed in the bath 3901.

Reference electrode 3908 is in a second bath 3907 which is in fluid connection with the first bath.

Referring to Fig. 25, substrate 4000 is patterned
20 such that interleaving fingers 4006 and 4008 are connected to electrodes 4002 and 4004, respectively. In this figure, metallization fingers 4006 will be the base for growth of the p-type legs 4010, and metallization fingers 4008 will be the base for growth of the n-type
25 legs 4012.

The substrate 4000 is patterned such that holes are left for growth of legs 4010 and 4012. However, each growth can occur successively without the need to cover

the previously grown legs. This is a significant manufacturing advantage over the first growth embodiment described above at least because it avoids the problem of double exposure of the photoresist.

Growth of the n-type or p-type legs may be selectively chosen, and growth of the other prohibited, by a careful choice of voltages for each of the electrodes. Fig. 26 shows a voltammogram of a general system. Growth of, e.g., n-type or p-type legs may occur at point 4106. No growth occurs at point 4102 and removal of the deposited film occurs at 4104. These are exemplary and depend on the system. In general, growth of an n-type or p-type leg may occur at point 4106 in the graph, and no growth occurs at 4102. Thus, the bipotentiostat may be set up with appropriate voltages such that growth occurs for the n-type but not for any other growth, e.g., one of the voltages is at point 4104 and the other is at 4102. The bath and voltage may then be changed so that growth occurs for the p-type but not for any other growth.

Variations of the this bipotentiostat technique may also be used. This can be done in two different ways:

1) only one bath, but two voltages results in two different compositions, one n-type the other p-type. This can be done with the bipotentiostat since it can control independently two separate electrodeposition voltage values (on the same substrate, provided that two

separate electrodes - one for n, one for p - are patterned on it), or

2) two baths but same configuration: in sequence, first bath, electrode 1 for n-type, electrode 2 at voltage so that no deposition takes place (zero current); then second bath, electrode 1 at zero current, electrode 2 for p-type.

Additional formation embodiments are shown in Fig. 27. Fig. 27A shows the first step of the process. A substrate 2700 of silicon/SiO₂ is first formed. This is formed with a thin conductor, approximately .5μm thick, of etchable conductive material 2702. The preferred material, for example, is TiAl. Copper pads 2704 and 2706 are formed on the thin conductor 2702 and are each covered with a diffusion barrier 2708, 2710 of a type previously discussed.

In Fig. 27B, a photoresist 2715 is formed which has first hole areas 2718. Each of these hole areas 2718 will be filled with an n-type material 2720. Note that the n-type material is formed to one side of each of the copper pads 2706, 2704, i.e., not centered over the pad. The n-type material is covered with a Ni diffusion barrier 2722 and a solder layer 2724 which is BiSn or PdSn. All of this can be done by electrochemical deposition.

Fig. 27C shows the next step of adding another, thin, photoresist layer 2730, and opening second

holes 2732 which will be used for the p-type material. This is preferably done under yellow light. The thin layer of photoresist 2730 covers the n-type material 2720. The layers of p-type material, and corresponding solder layers, are formed in those holes.

Fig. 27D shows dissolving the photoresist 2715, 2730, and the metallization between the resultant legs in the area 2740 to avoid a short circuit between all of the legs. This is done using an acid etch, for example. A top substrate is added to form interconnections 2744 between the adjacent n- and p-layers.

An alternative formation technique, which we call an interdigitated technique, is described with reference to Fig. 28. This begins by forming a substrate with metal "fingers." The substrate is shown in cross-section in Fig. 28A, and is shown from above in Fig. 28B. Further detail blow-up of the fingers is shown in Fig. X2C. As can be seen from this figure, each of the fingers is formed with increased size rounded parts on each finger 2800. According to this technique, one of the legs will be formed at each round part 2802, 2804.

The process carries on using the techniques shown in Fig. 28D. First, as in the above technique, a photoresist 2810 with holes 2812 is added. The first hole over a first portion of the finger is filled with n-type material 2820 as shown in Fig. 28E. This is done

in an n-type electrolyte where the p-type fingers are biased positive to prevent deposition.

5 Subsequently, as shown in Fig. 28F, the p-type ECD is carried out in a p-type electrolyte. During this time, the n-type electrodes are biased positive in order to prevent their deposition. This results in n- and p-legs which are adjacent to one another.

10 Fig. 28G shows depositing a thin layer of metallization 2840 to the tops of the n- and p-legs. This also has an undesired effect of adding excess metallization on top of the photoresist 2810.

15 In Fig. 28H, the photoresist is removed by conventional techniques, e.g., dipping the entire substrate into acetone.

20 A top substrate is then attached as shown in Fig. 28I. At this time, the bottom substrate is removed to remove the otherwise short circuit that would exist between all the legs. A new bottom substrate is interconnected as shown in Fig. 28J, which includes new bus portions bonded to the legs as shown in Fig. 28K. The interconnection can be, for example, as shown in Fig. 28L.

25 In summary, a thermoelectric device has been developed which may advantageously be employed for powering small consumer electronics such as watches. N-type legs of significant thickness are deposited using materials such as BiTe alloys. Such legs may be

deposited at high deposition rates, meaning that only two to three hours may be needed for 40 micrometer-thick legs. Changes in stoichiometry and surface morphology are well understood. P-type layers of $(\text{Bi}_{1-x}\text{Sb}_x)_2\text{Te}_3$ layers have also been deposited using increased Sb solubility achieved by using tartaric acid. This has resulted in a vast improvement in deposition rate and surface morphology, resulting in less sponge-like deposits.

Diamond substrates (100 μm to 1 mm thick) can be obtained from a number of commercially available sources (e.g., Norton, Diamonex, Crystalline Materials, and General Electric). Materials other than diamond which may be used include: high purity silicon, aluminum nitride, or materials with similar properties available from, e.g. Carborundum, Inc.

The performance of the device depends on the size of the thermoelectric legs, the number of legs, the temperature difference across the legs, the electrical contact resistance between these legs and the upper and lower stack structures, and the thermal resistance between the heat-dissipating device and the substrate.

A useful amount of electrical power for a thermoelectric device to produce to power an electronic device may be on the order of several tens to hundreds of microwatts at one volt in low ΔT environments.

EXAMPLE

A wristwatch application is described as an example. It should be noted that any electronic device with similar power requirements may be powered similarly, as long as a thermal gradient is present.

ΔT may be as low as 1°C for a wristwatch application. This low ΔT is assumed as an operating point due to uncertainty in the ambient environment and the efficiency of heat rejection. A desirable size for the thermoelectric device module may be in the range of about 1.5 mm x 1.5 mm in such an application.

A basic heat collection area of 100 mm^2 is considered (e.g., 10 mm x 10 mm) for purposes of this discussion. Heat rejection occurs from the outer edge of the watch front, or the face (the center is typically glass). Thus, it may be desirable for the thermoelectric device to be positioned around the circumference of the watch interior, drawing heat from the solid back, and rejecting heat to the periphery of the front side.

A thermal analysis of one potential watch configuration has been performed. This analysis identifies the design operating temperature and a thermal resistance budget for the thermoelectric device. One complication for the analysis is a large variation in the ambient environment for heat rejection (i.e., the

air temperature and humidity) and the type of clothing being worn. An additional variable is the amount of time a watch is worn each day. Thermal and structural models may be used to determine the optimum configuration of the device under various operating conditions. Considerations include the thermal resistance, heat spreading, and the leg configuration. Considerations for mechanical stress should further include device failure due to thermal cycling.

One possible design temperature differential identified by the analysis is 1°C . Using a figure of merit of $200\ \mu\text{V}/^{\circ}\text{C}$ per BiTe leg, the thermoelectric device power source would require 5000 legs for the design temperature differential of 1°C to produce the one volt (open circuit) required to run the watch.

The thermal resistance budget depends on the conduction paths for the heat flow from a watch back to a front surface 55. These include thermoelectric device elements θ_{TEG} , air resistance within the watch θ_a , skin contact resistance θ_s , a heat transfer resistance to the ambient air θ_o , a heat conduction resistance of other internal watch parts θ_p , and a contact resistance with the thermoelectric device θ_c .

As is known, resistance $[\text{K}/\text{W}]$ is inversely proportional to conductance $[\text{W}/\text{K}]$, and conductance

equals conductivity times area divided by length
[W/m-K]:

$$\theta = \frac{1}{\lambda} = \frac{L}{\lambda_0 s}$$

5 For the watch,

$$\theta = \theta_0 + \left(\frac{1}{\theta_p} + \frac{1}{\theta_a} + \frac{1}{\theta_c + \theta_{TEG}} \right)^{-1} + \theta_s$$

10 Fig. 4 shows a detail of the circumferential
configuration of a watch body, which represents the
major contribution to parallel heat flow. This
configuration has a height h , a radial width w , and a
radius (to the center of width w) of r . E.g., h may be
15 about 4 mm, r about 20 mm, and w about 3 mm. Assuming a
plastic body, λ_{plastic} is about 0.2 W/m-K, and θ_p is about
50 K/W. In this analysis, values of θ_a of about 100 K/W
and $\lambda_{\text{Bi-Te}}$ of about 1.5 W/m-K were also used. In the case
of $\lambda_{\text{Bi-Te}}$, a θ_{TEG} of about 50 K/W was obtained.

20 From this analysis, a thermal resistance budget for
the thermoelectric device element was established at a
value of 50 K/W (equivalently, 50°C/W). This thermal
resistance budget can be used to evaluate candidate
thermoelectric device configurations which produce the

required voltage and power and have an acceptably high thermal resistance.

Although only a few embodiments have been described in detail above, those having ordinary skill in the art will certainly understand that many modifications are possible in the preferred embodiment without departing from the teachings thereof. All such modifications are intended to be encompassed within the following claims. E.g., other materials can be substituted for the BiTe alloy-based material to achieve different performances and temperature ranges. Some suitable materials exhibit a ZT value greater than 1, where ZT is a figure of merit defined as:

$$ZT = \frac{ST^2}{(\rho \cdot k)}$$

where S is the material's Seebeck coefficient, ρ is the electrical resistivity, and k is the thermal conductivity. In general, however, this depends on the application. For example, such a criterion may not be applicable for waste heat recovery systems, etc.

In other embodiments, each of the materials listed in Table I may be replaced with another material having suitable electronic, thermal, and mechanical properties and substituted into the power-generating device. The structures of the upper and lower stack structures can also be modified.

High-thermal conductivity materials, such as silicon carbide, or related materials, such as aluminum nitride, boron nitride, or beryllium oxide have properties close to those for diamond. In general, these materials are electrical insulators, have high thermal conductivities, and are durable. Other materials having desirable thermal, mechanical, and electrical properties, such as ceramics or polymers, may also be used.

Thermoelectric BiTe alloy-based alloys can also be deposited as a film using the flash-evaporation method. In this technique, the BiTe alloy-based material, in the form of fine grains, is fed into a high-temperature heating chamber. The chamber is then evacuated and heated to the desired temperature. N-type BiTe alloys can be grown by introducing an additional chalcogen source, such as tellurium or selenium, into the heating chamber. The stoichiometric amount of chalcogen can be varied by adjusting the temperature (and thus the vapor pressure) of the source material. Similarly, p-doped films can be grown by introducing additional bismuth, antimony, or tellurium to the source material, and by adjusting the temperature accordingly. Films having thicknesses on the order of a 10-20 μm can be formed with this method.

The techniques can also be used to form nanowires by using electro-deposition for filling porous templates

with nanotube structures. Low dimensionality thermoelectric materials will likely have better performance due to quantum effects and interface transport effects for electrical and thermal transport parameters.

Still other embodiments are within the scope of the following claims.

What is claimed is:

1. A thermoelectric device using a temperature differential between a first higher temperature surface and a second lower temperature surface to generate power, comprising:

a high thermal conductivity and high electrical resistivity substrate in thermal coupling with the first higher-temperature surface, coupled such that heat flows between the high temperature surface and the substrate; and

at least 1000 thermoelectric legs, each said thermoelectric leg comprising:

a thermoelectric film material in thermal couple with the substrate; and

a multilayer structure disposed between the substrate and the thermoelectric material, the multilayer stack structure comprising thermally and electrically conductive layers for supplying heat between the substrate and the thermoelectric material and also conducting current from the thermoelectric material,

wherein at least a plurality of said at least 1000 thermoelectric legs are electrically in series and thermally in parallel.

1 2. The device of claim 1, wherein the
2 thermoelectric material is a thermoelectric film
3 deposited onto the multilayer stack structure.

1 3. The device of claim 1, wherein said multilayer
2 structure including at least one conductive layer formed
3 of a material that has a high solid state solubility,
4 and including a barrier layer between said conductive
5 layer and said thermoelectric material which prevents
6 said material from dissipating into said thermoelectric
7 material.

1 4. The device of claim 1, wherein the legs
2 comprise a series of alternating p- and n-doped regions.

1 5. The device of claim 4, wherein each of the p-
2 doped and n-doped regions in the alternating series are
3 electrically connected in groups of legs such to match a
4 predetermined circuit.

1 6. The device of claim 1, wherein the
2 thermoelectric material is Bi_2Te_3 , or a Bi_2Te_3 -based alloy.

1 7. The device of claim 1, wherein the electrical
2 component is an electrical watch.

1 8. The device of claim 1, wherein the
2 electrically insulating, high thermal conductivity
3 material is selected from the group consisting of
4 diamond, silicon carbide, boron nitride, alumina,
5 aluminum nitride, high resistivity silicon or beryllium
6 oxide.

1 9. The device of claim 1, wherein the stack
2 structure comprises a metallic layer attached directly
3 to the diamond or high thermal conductivity substrate.

1 10. The device of claim 9, wherein the stack
2 structure further comprises a diffusion barrier layer
3 for separating the metallic layer from the
4 thermoelectric material.

1 11. The device of claim 9, wherein the stack
2 structure comprises:

3 a metallization layer attached to a surface of the
4 diamond or high thermal conductivity substrate;

5 an outer diffusion barrier layer attached to the
6 metallization layer;

7 an electrically conducting layer formed of a
8 material having a high solid state solubility, attached
9 to the diffusion barrier layer;

10 an inner diffusion barrier layer attached to the
11 electrically conducting layer; and

12 a contact layer attached to the inner diffusion
13 barrier layer.

1 12. The device of claim 4, wherein each of the p-
2 doped and n-doped regions in the alternating series has
3 a thickness in an range between 5 μm and 200 μm .

1 13. The device of claim 4, wherein the p-doped
2 region and n-doped region are coupled with each other
3 via the multilayer stack structure.

1 14. The device of claim 9, wherein the stack
2 structure comprises:

3 a metallization layer attached to a surface of the
4 diamond or high thermal conductivity substrate;

5 a contact layer attached to the thermoelectric film
6 material; and

7 an electrically conducting layer disposed between
8 the metallization layer and the contact layer.

1 15. The device of claim 1, wherein a growing
2 direction of the deposited thermoelectric material is a
3 heat supplying direction.

1 16. A microfabricated microgenerator for powering
2 an electronic component using a temperature differential
3 between a hot region and a cool region, comprising:

4 a diamond or high thermal conductivity and low
5 electrical conductivity substrate in thermal couple with
6 the hot region;

7 a thermoelectric material in thermal couple with
8 the substrate; and

9 a stack structure disposed between the substrate
10 and the thermoelectric material, the stack structure
11 comprising:

12 a metallization layer attached to a surface of the
13 substrate;

14 an outer diffusion barrier layer attached to the
15 metallization layer;

16 an electrically conducting layer attached to the
17 diffusion barrier layer;

18 an inner diffusion barrier layer attached to the
19 electrically conducting layer; and

20 a contact layer attached to the inner diffusion
21 barrier layer.

1 17. A method of fabricating p-type thermoelectric
2 film having a controlled composition and morphology
3 using electrodeposition, comprising:

4 providing a solution including a mixture of
5 bismuth, antimony, and tellurium in an acid solution;

6 disposing a substrate on which the film is to be
7 deposited within the solution;

8 disposing a counter-electrode within the solution;
9 and
10 providing a voltage across the substrate and the
11 reference-electrode of between about -10 to -200 mV.

1 18. The method of claim 17, wherein the acid is
2 nitric acid.

1 19. The method of claim 17, wherein the acid is
2 hydrochloric acid.

1 20. The method of claim 17, wherein the acid is
2 sulfuric acid.

1 21. The method of claim 17, wherein the mixture
2 further comprises selenium.

1 22. The method of claim 17, wherein the acid
2 further comprises tartaric acid.

1 23. A diffusion barrier for use between a
2 thermoelectric material and a metal, comprising a film
3 of $Ta_{40}Si_{14}N_{46}$.

1 24. A method of making a diffusion barrier for use
2 between a thermoelectrical material and a metal,
3 comprising:

4 evacuating a sputtering chamber to a vacuum on the
5 order 10^{-7} mbar;

6 flowing an argon-containing gas and a nitrogen-
7 containing gas into the chamber to a pressure on the
8 order of a few mbar;

9 disposing a TaSi target within the chamber; and
10 exciting a plasma within the chamber.

1 25. A method of fabricating an n-type
2 thermoelectric film having a controlled composition and
3 morphology using electrode position, comprising:

4 providing a solution including a mixture of bismuth
5 and tellurium in an acid having a pH of about zero range
6 -1 to +1 pH;

7 disposing a substrate on which the film is to be
8 deposited within the solution;

9 disposing a counter-electrode within the solution;
10 and

11 providing a voltage across the substrate and the
12 reference electrode of between about -200 to 0 mV.

1 26. The method of claim 25, wherein the acid is
2 sulfuric acid.

1 27. The method of claim 25, wherein the mixture
2 further comprises selenium.

1 28. The method of claim 25, wherein the acid
2 further comprises tartaric acid or EGTA or EDTA.

1 29. A method of fabricating n- and p-type
2 thermoelectric legs on a substrate having a controlled
3 composition and morphology using electrodeposition,
4 comprising:

5 providing a solution including a mixture of
6 thermoelectric elements in an acid having a pH of
7 between about -1 and +1;

8 disposing a metalized substrate, a first working
9 electrode, on which the film is to be deposited within
10 the solution;

11 disposing a second working electrode;

12 disposing a counter-electrode; and

13 providing voltages between the counter-electrode
14 and the second working electrodes with a bipotentistat
15 such that electrodeposition of an n-type material occurs
16 on the first working electrode; and

17 providing voltages across the counter-electrode and
18 the second working electrode with the bipotentistat such
19 that electrodeposition of a p-type material occurs on
20 the substrate.

1 30. A method as in claim 29, wherein the n- and p-
2 substrates are formed in the same solution.

1 31. The method of claim 29, wherein the n- and p-
2 substrates are formed in two different solutions.

1 32. The method of claim 29, wherein the acid is
2 sulfuric acid, hydrochloric acid, and/or nitric acid.

1 33. The method of claim 30, wherein the acid
2 further comprises tartaric acid, EGTA, and/or EDTA.

1 34. The method of claim 31, further comprising the
2 steps of monitoring the current with a current monitor,
3 and stopping the deposition at a predetermined
4 transition point to reduce the occurrence of mushroomed
5 legs.

1 35. The method of claim 29, further comprising the
2 steps of monitoring the current with a current monitor,
3 and reversing the polarity of the working and counter
4 electrodes at a predetermined transition point, whereby
5 to control the film thickness or to flatten the tops of
6 the legs.

1 36. The method of claim 29, further comprising the
2 steps of monitoring the current with a current monitor,
3 and decreasing the potential between the working and
4 counter electrodes at a predetermined transition point,
5 whereby to control the film thickness.

1 37. The method of claim 23, wherein the mole ratio
2 of Bi:Sb:Te is such that films result with $\text{Bi}_{1-x}\text{Sb}_x\text{Te}_3$ and
3 $1.5 \leq x \leq 1.8$.

1 38. A method of fabricating a structure on a
2 substrate with first and second conductivity type legs,
3 comprising:
4 depositing a metallic film on the substrate;
5 patterning a photoresist on the metallic film;
6 electrodepositing a first conductivity type
7 material on the metallic film to form legs of a first
8 conductivity type;
9 covering the first conductivity type material with
10 a protective layer;
11 patterning a photoresist on the deposited layers;
12 electrodepositing a second conductivity type
13 material on the deposited layers to form legs of a
14 second conductivity type.

1 39. The method of claim 38, further comprising
2 depositing an underfill material between the legs.

1 40. The method of claim 38, further comprising
2 processing the photoresist using yellow light.

1 41. The method of claim 38, wherein a thick
2 photoresist technique is used to deposit the
3 photoresist, the thick photoresist technique including:
4 depositing a first layer of photoresist;
5 patterning the first layer;
6 depositing a second layer of photoresist; and
7 patterning the second layer.

1 42. The method of claim 41, further comprising
2 ultrasonically agitating the photoresist in water.

1 43. A method of forming a thermoelectric device,
2 comprising:

3 obtaining an interconnect bus pattern on a
4 substrate, said interconnect bus pattern connecting
5 between at least a first area on said substrate and a
6 second area on said substrate;

7 using an electrical deposition process to grow a
8 first semiconductor material having thermoelectric
9 properties and having a first conductivity type on said
10 first area;

11 using an electrical deposition process to grow a
12 second semiconductor material having thermoelectric
13 properties on said second area, said second
14 semiconductor material on said second area having a
15 different conductivity type than said first
16 semiconductor material on said first area; and

17 connecting said first and second thermoelectric
18 devices in series with one another via the interconnect
19 bus pattern already on the substrate, to produce an
20 output voltage from the series combination of said first
21 and second semiconductor materials, based on a
22 temperature gradient thereacross.

1 44. A method as in claim 43 wherein said materials
2 are grown using electro-chemical deposition.

1 45. A method as in claim 43 wherein said materials
2 are grown using molecular beam epitaxy.

1 46. A method as in claim 43 wherein said
2 semiconductor materials formed on said first and second
3 areas comprise thermoelectric legs, and said
4 thermoelectric legs are between 5 and 100 μm in
5 thickness.

1 47. A method as in claim 46 wherein said first
2 semiconductor material is an n-type material and said
3 second semiconductor material is a p-type material.

1

2 48. A method as in claim 44 wherein said electro-
3 chemical deposition comprises:

4 obtaining said contact layer,

5 forming a photoresist on areas defining a desired
6 pattern for the semiconductor material and applying
7 electrical current to cause material to be electro-
8 chemically deposited on the substrate based on said
9 desired pattern.

1 49. A method as in claim 48 wherein said material
2 includes BiTe alloys.

1 50. A method as in claim 49 wherein said material
2 includes an electrolyte including an acidic composition
3 of bismuth, antimony, tellurium, and selenium materials
4 soluble in said acids.

1 51. A method as in claim 43 wherein said substrate
2 is a heat conducting but electrically insulating
3 substrate.

1 52. A method as in claim 48 wherein said
2 photoresist is deposited on said substrate to a
3 thickness of a desired height of the thermoelectric
4 element.

1 53. A method as in claim 52, further comprising
2 forming columnar holes to form columnar semiconductor
3 material.

1 54. A method as in claim 52 wherein applying said
2 photoresist comprises:
3 depositing a photoresist to a desired thickness of
4 a height of the thermoelectric element; and
5 etching holes in the photoresist at a pattern
6 corresponding to locations of a first conductivity type
7 of thermoelectric elements, said holes corresponding to
8 a pattern of an interconnect bus on the substrate.

1 55. A method as in claim 43 wherein said
2 interconnect bus is formed of copper.

1 56. A method as in claim 55 further comprising a
2 diffusion layer to prevent the copper from diffusing
3 into the thermoelectric material.

1 57. A method as in claim 11, further comprising
2 forming a conductive layer of a material which has a
3 high solid-state solubility and forming an
4 interdiffusion barrier layer between said material and
5 said thermoelectric material.

6 58. A method of forming a thermoelectric device,
7 comprising:

8 depositing a photoresist on a substrate to a
9 thickness of a desired height of the thermoelectric
10 element, with at least first and second openings
11 therein;

12 depositing a first semiconductor material having
13 thermoelectric properties and having a first
14 conductivity type in said first opening;

15 depositing a second semiconductor material having
16 thermoelectric properties in said second opening, said
17 second semiconductor material on said second area having
18 a different conductivity type than said first
19 semiconductor material on said first area; and

20 connecting said first and second thermoelectric
21 devices in series with one another to produce an output
22 voltage from the series combination of said first and
23 second semiconductor materials, based on a temperature
24 gradient thereacross.

1 59. A method as in claim 58 wherein applying said
2 photoresist comprises depositing a photoresist to a
3 desired thickness of a height of the thermoelectric
4 element;

5 etching holes in the photoresist at a pattern
6 corresponding to locations of a first conductivity type
7 of thermoelectric elements.

1 60. A method as in claim 59, wherein said holes
2 are columnar.

1 61. A method as in claim 58 wherein said holes
2 correspond to a pattern of an interconnect bus on the
3 substrate.

1 62. A system as in claim 43 further comprising a
2 conductive layer formed of a material which has a high
3 solid-state solubility and an interdiffusion barrier
4 layer over said material.

1 63. A system as in claim 58 further comprising a
2 conductive layer formed of a material which has a high
3 solid-state solubility and an interdiffusion barrier
4 layer over said material.

1 64. A method of forming a plurality of series-
2 connected thermoelectric elements, comprising:
3 obtaining a substrate with a conductive
4 interconnect bus pattern formed thereon;
5 covering a portion of said substrate with a mask;
6 growing thermoelectric elements on portions of said
7 substrate that are not covered by said mask, using IC
8 fabrication techniques, thereby using at least part of

9 the existing interconnect device to connect to the
10 thermoelectric device.

1 65. A method as in claim 64, wherein said
2 thermoelectric portions are columnar.

1 66. A method as in claim 65 wherein said forming
2 comprises first forming n-type thermoelectric devices
3 on a first group of interconnect patterns, and second
4 forming second thermoelectric devices on a second group
5 of interconnect patterns.

1 67. A method of forming a thermoelectric device,
2 comprising:
3 forming a conductor substrate;
4 forming a resist, defining portions on the
5 conductor substrate where deposits are not desired to be
6 located, a thickness of said photoresist being
7 substantially a desired height of a thermoelectric
8 material;

9 forming holes in the resist; and
10 forming the thermoelectric materials in said holes
11 which are electrically and thermally coupled to said
12 conductor substrate.

1 68. A method as in claim 67 further comprising
2 first forming one of n- and p-legs, masking said one of

3 n- and p-legs, second patterning said photoresist to
4 form second holes spaced from said first holes, and then
5 forming the other of said n- and p-legs in said second
6 holes.

1 69. A method as in claim 66 wherein said
2 photoresist is substantially 40 μm in thickness.

1 70. A method as in claim 67 wherein said holes are
2 formed using a photomask, and further comprising
3 shifting said photomask with an aligner.

1 71. A method as in claim 67 further comprising
2 patterning the conductive substrate.

1 72. A method as in claim 67 wherein said substrate
2 is patterned into a desired pattern, and said legs are
3 formed on said desired pattern.

1 73. A method as in claim 66 further comprising
2 bonding a top substrate onto an opposite end of said
3 materials.

1 74. A method as in claim 67 further comprising
2 removing the bottom substrate, and bonding a bottom
3 metallization substrate thereon.

1 75. A method of forming n- and p-type material
2 on a single substrate, comprising:

3 obtaining a substrate;

4 forming a series of conductive patterns on the
5 substrate;

6 forming an n-type thermoelectric material on one
7 portion of said patterns, and

8 forming p-type thermoelectric materials on the
9 other portions of said patterns.

1 76. A method as in claim 75 wherein one of said n-
2 type and p-type is formed first, and the other of said
3 n-type and p-type is formed second, said other materials
4 which are formed second are formed without covering the
5 one material which is formed first.

1 77. A method as in claim 76 wherein the growth is
2 selectively controlled by selecting voltages which
3 allows one type to grow and prohibits the other type
4 from growing.

1 78. A thermoelectric device, comprising:

2 a plurality of n-type thermoelectric devices,
3 having first and second ends with a temperature gradient
4 thereacross;

5 a plurality of p-type thermoelectric devices, also
6 having first and second ends with the same temperature
7 gradient thereacross;

8 each of said n- and p-type thermoelectric legs
9 being 40 μm in thickness or less;

10 a first series connection between a first end of
11 said first n-type device and said first end of said
12 first p-type device and a second series connection
13 between said second end of said first p-type device, and
14 a second end of a second n-type device, to thereby place
15 at least a plurality of p- and n-type devices in series
16 with one another, maintaining a thermal parallel
17 relationship.

1 79. A device as in claim 77 wherein said
2 connections are connected by a solder bump.

1 80. A device as in claim 77 wherein there are more
2 than 1000 of said legs.

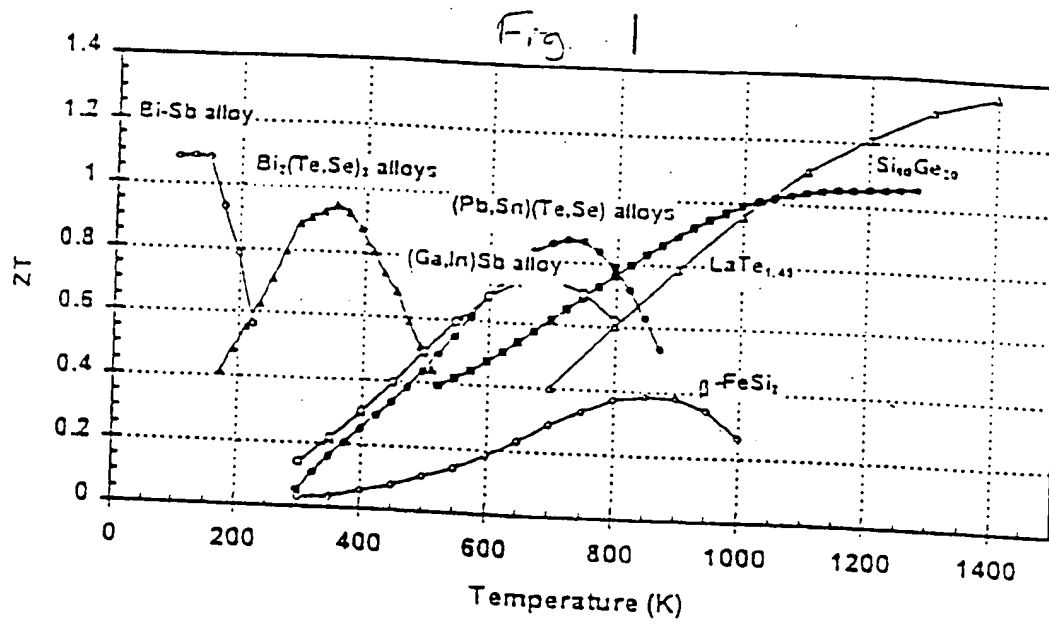
3 81. A device as in claim 77 wherein there are more
4 than 10,000 of said legs.

5 82. A device as in claim 77 further comprising a
6 first diffusion barrier at said first end of each of
7 said n-type devices and said p-type devices, and a
8 second diffusion barrier at a second end of each of said
9 n-type device and p-type device.

1 83. A method of forming a thermoelectric device,
2 comprising:

3 first forming an n-type BiTe alloy using electro-
4 chemical deposition to form a first leg, and second
5 forming a second leg of a p-type BiTe alloy; and

6 attaching one end of one of said materials to said
7 one end to the other of the materials, and operating
8 said materials such that they are thermally in parallel
9 but electrically in series.



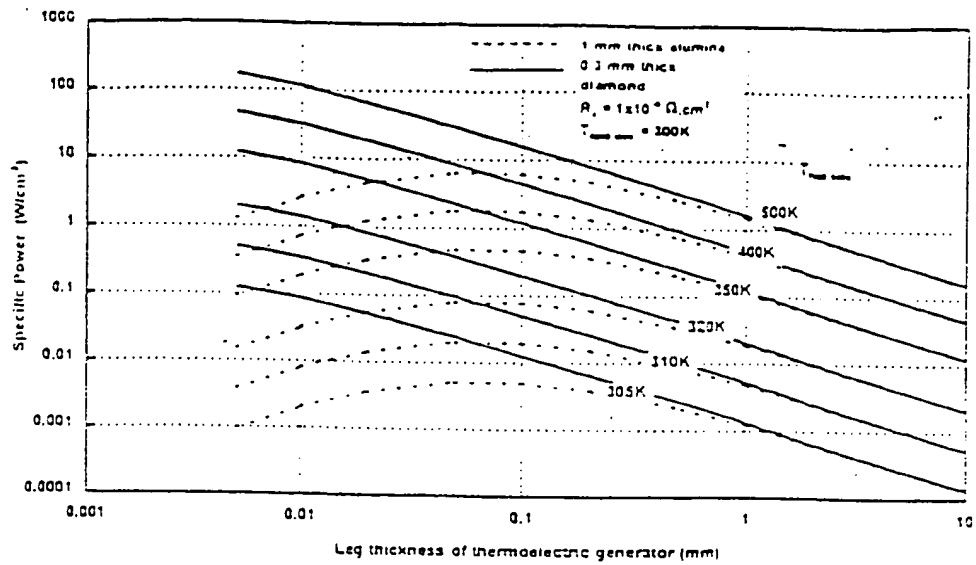
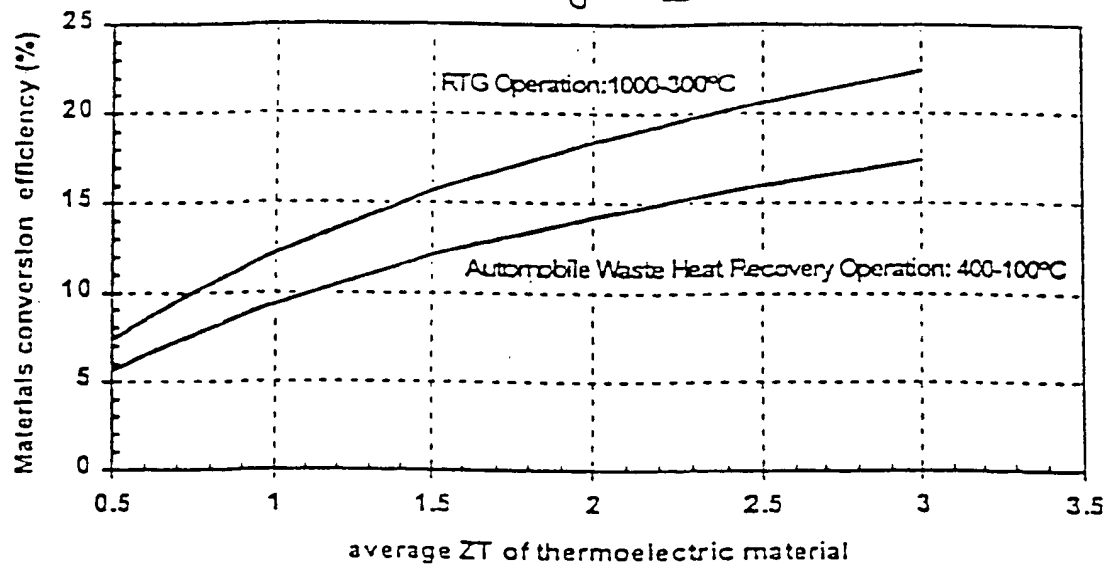


Fig. 2

Fig. 3



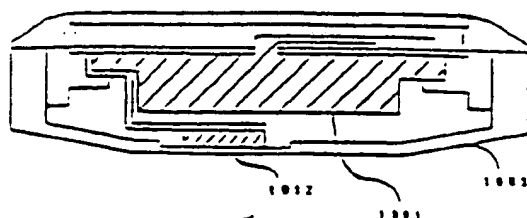
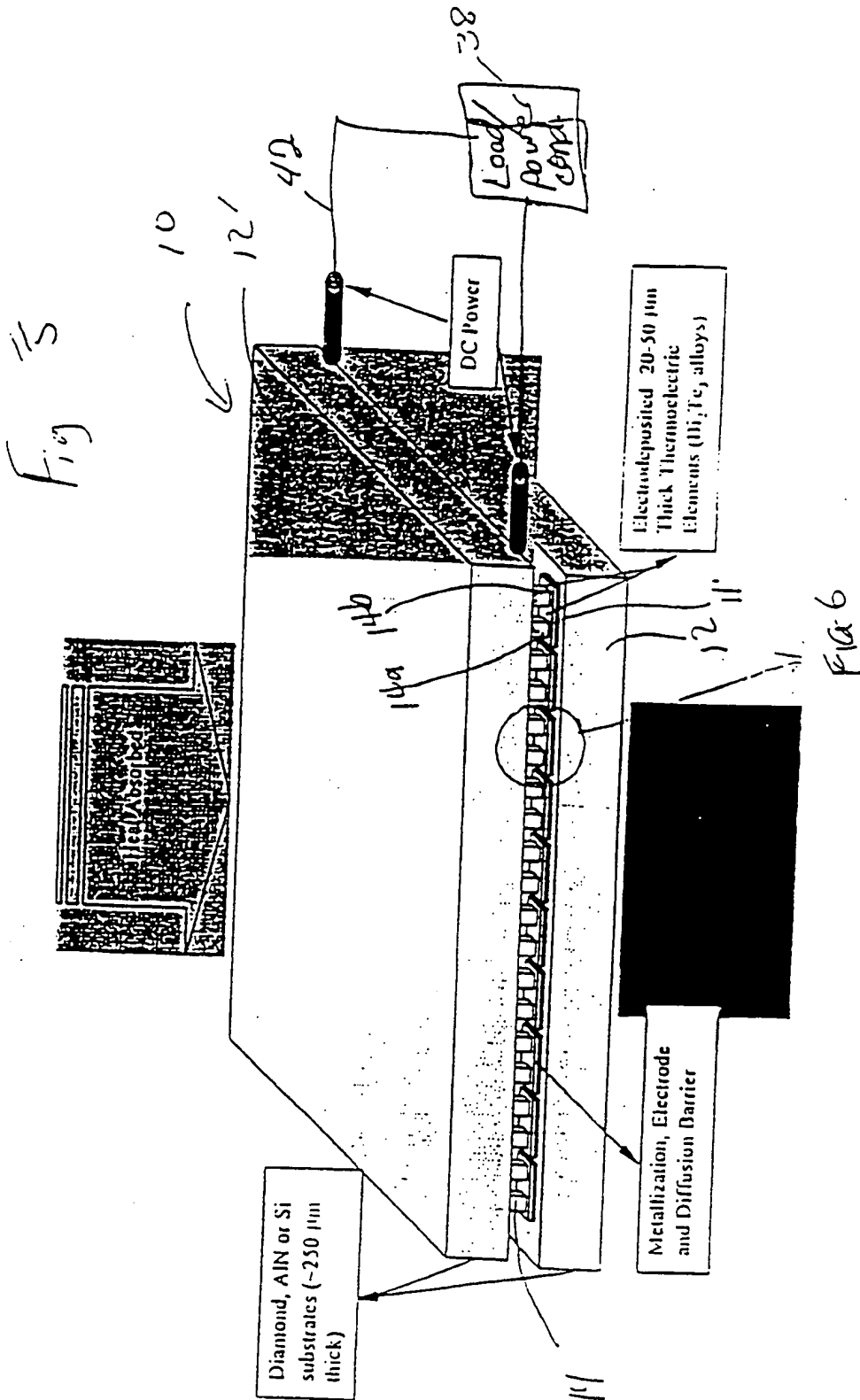


Fig 4

- 1001 thermoelectric device
- 1002 skin abutting surface
- 1003 time keeping circuit



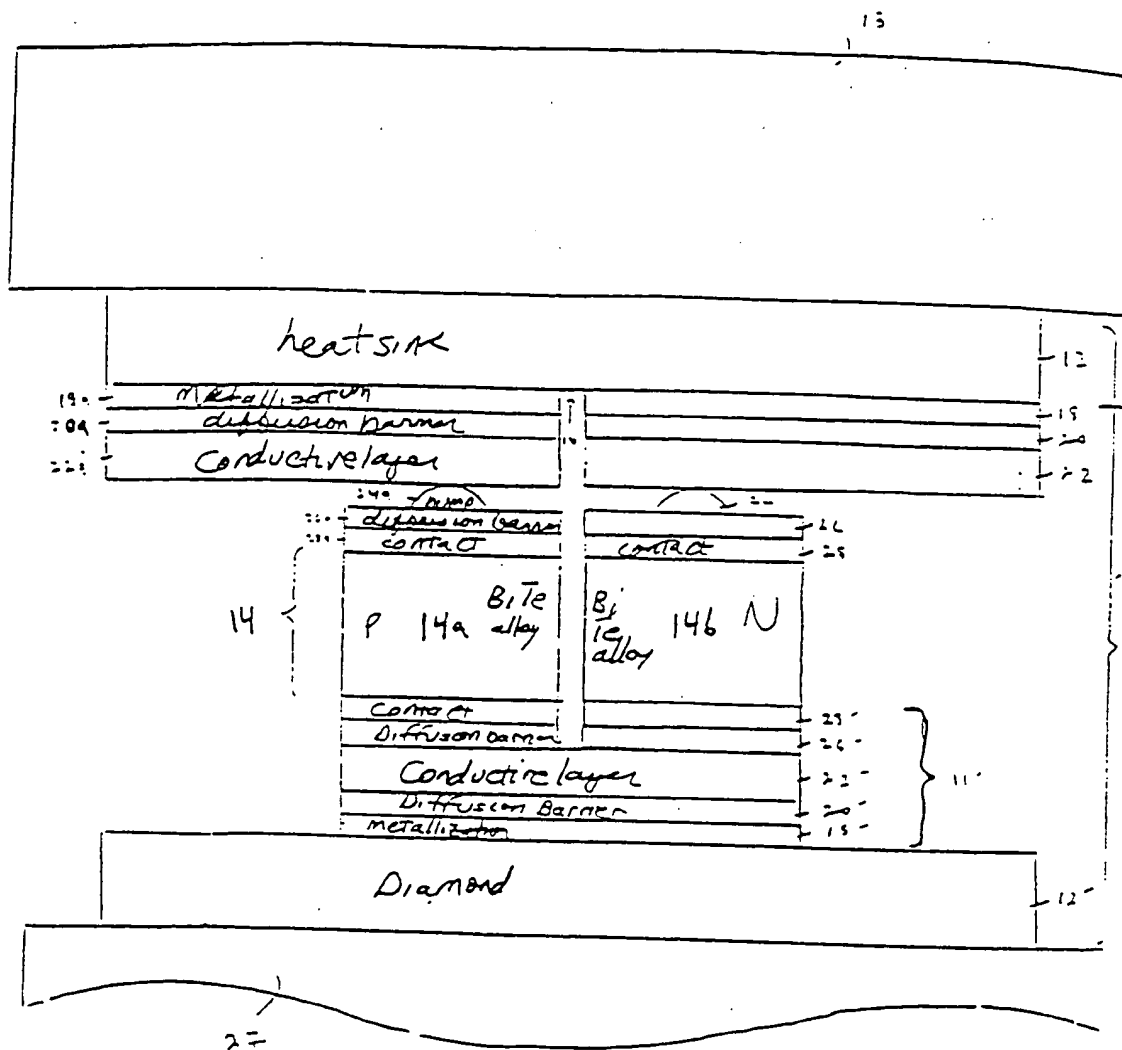


Fig.

6

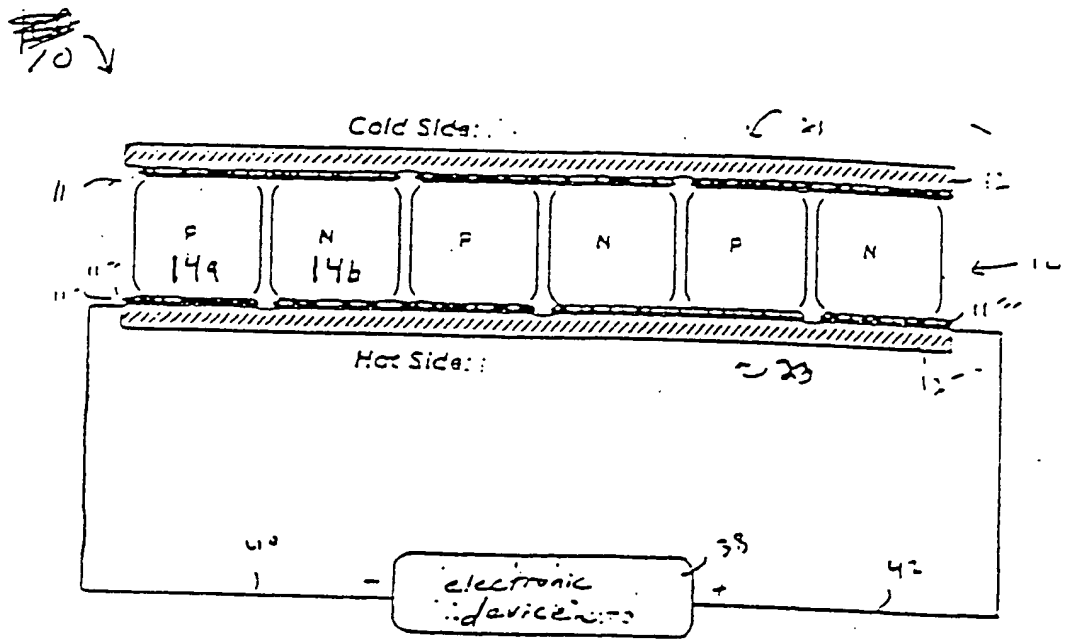
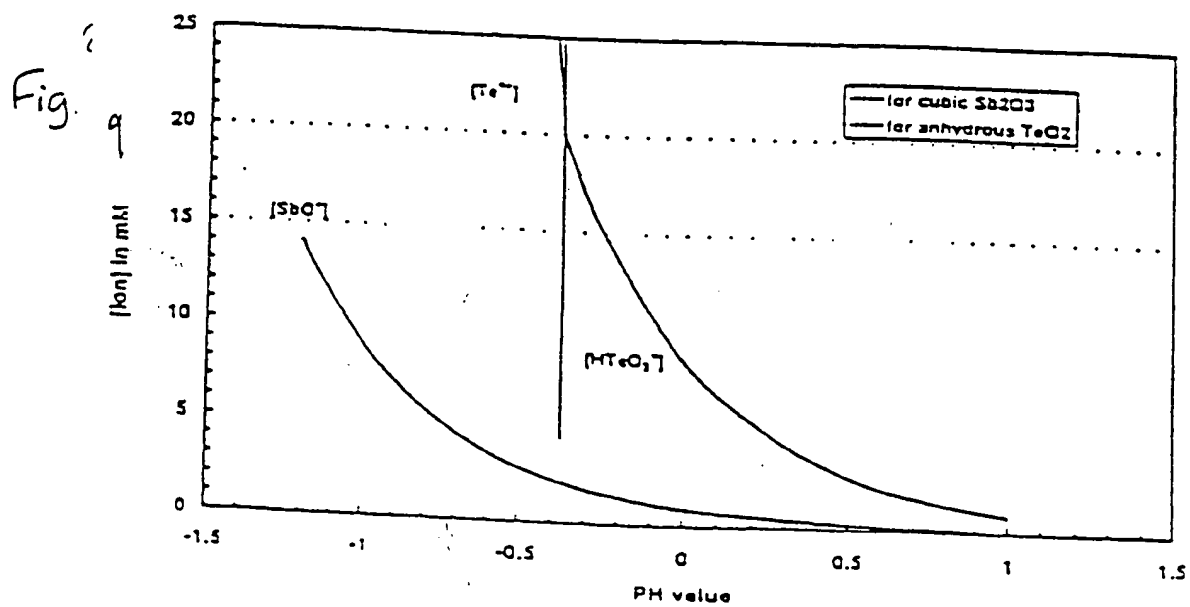
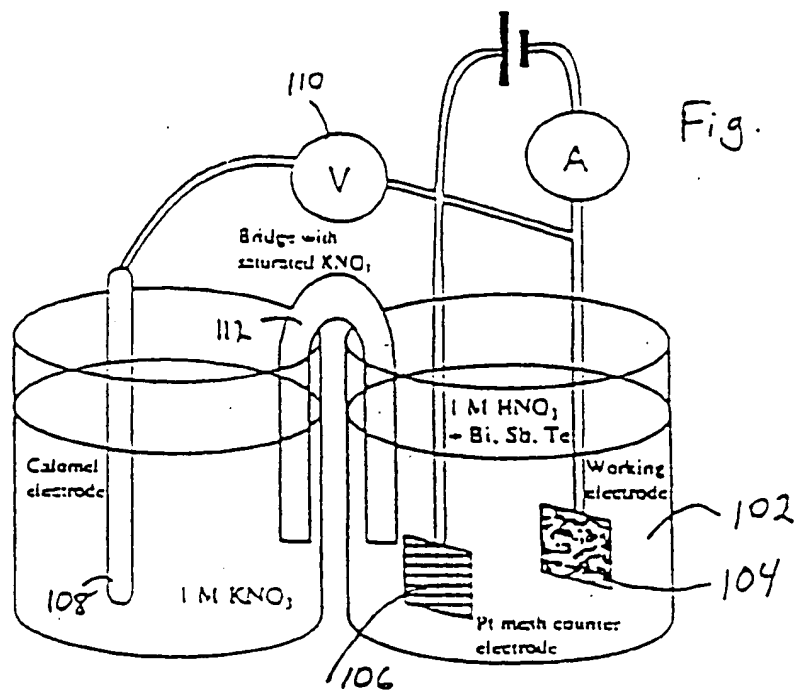


Fig.

7



JPL

Voltammogram of Bi and Te on Platinum

7 mM [Bi]; 10 mM [Te] in 1 M HNO₃
Pt Working and Counter Electrodes

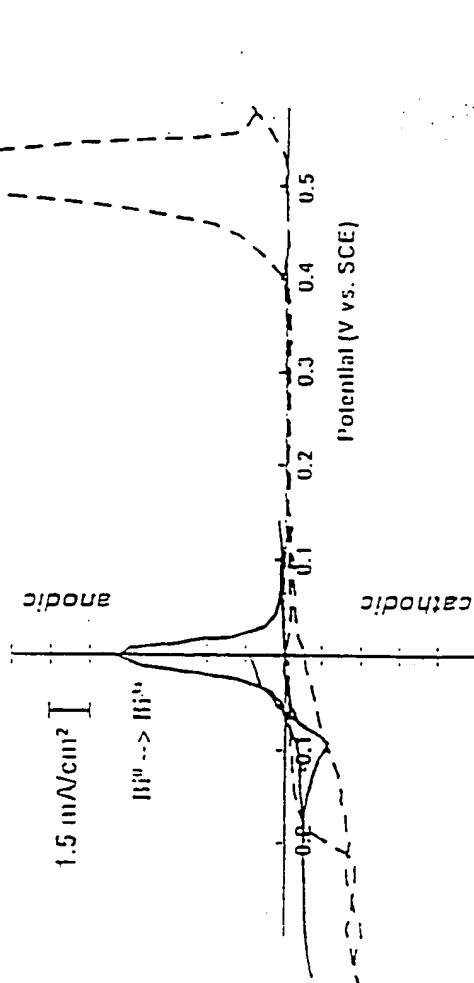
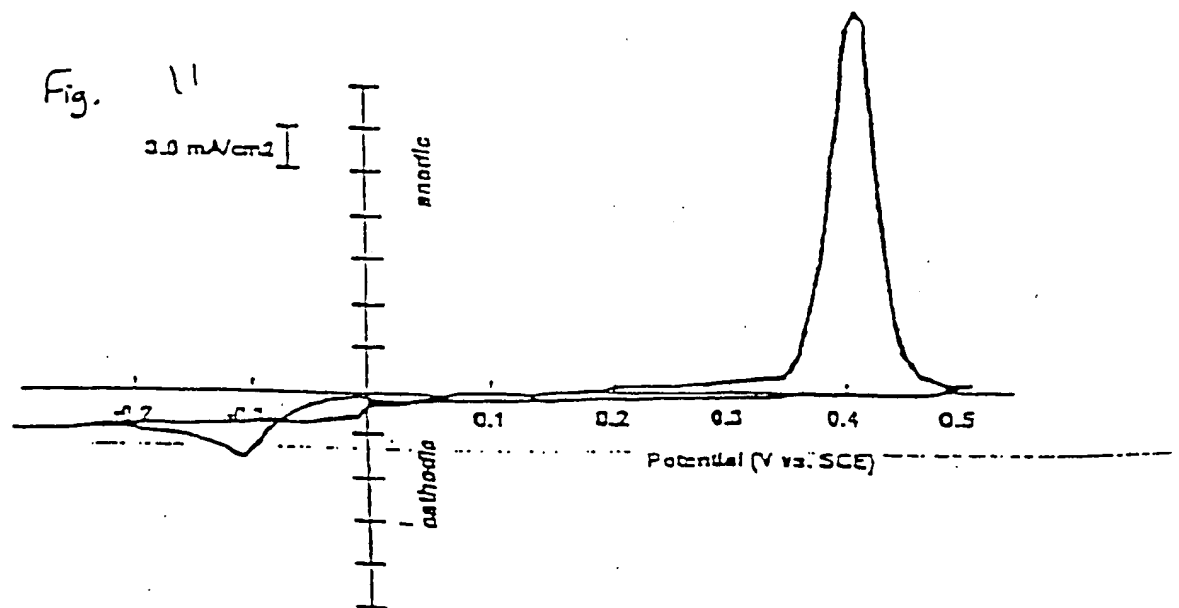


Fig. 10

ICT98 Nagoya Trade & Industry Center

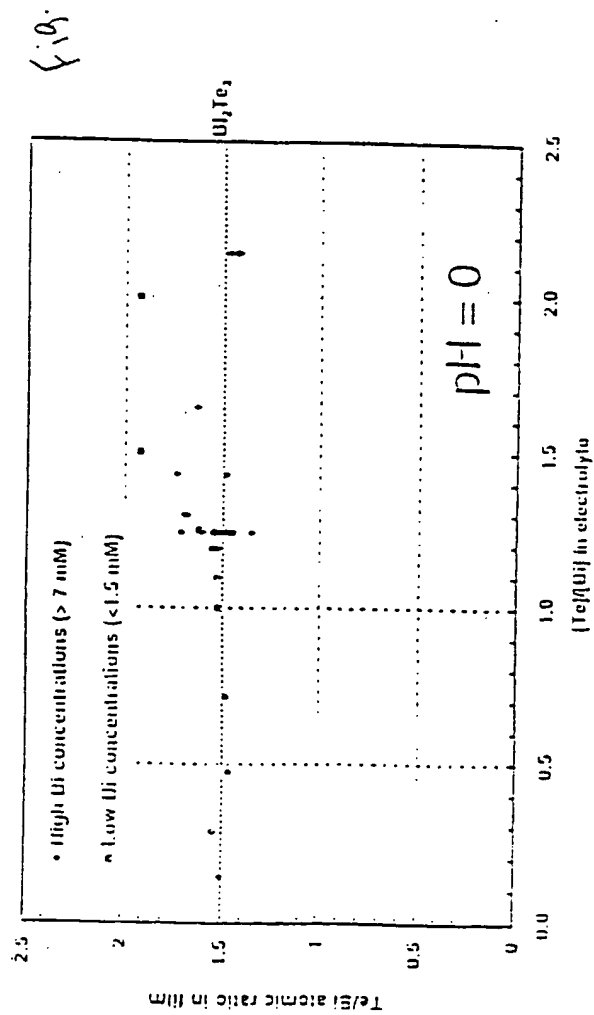
Slide 10



JPL

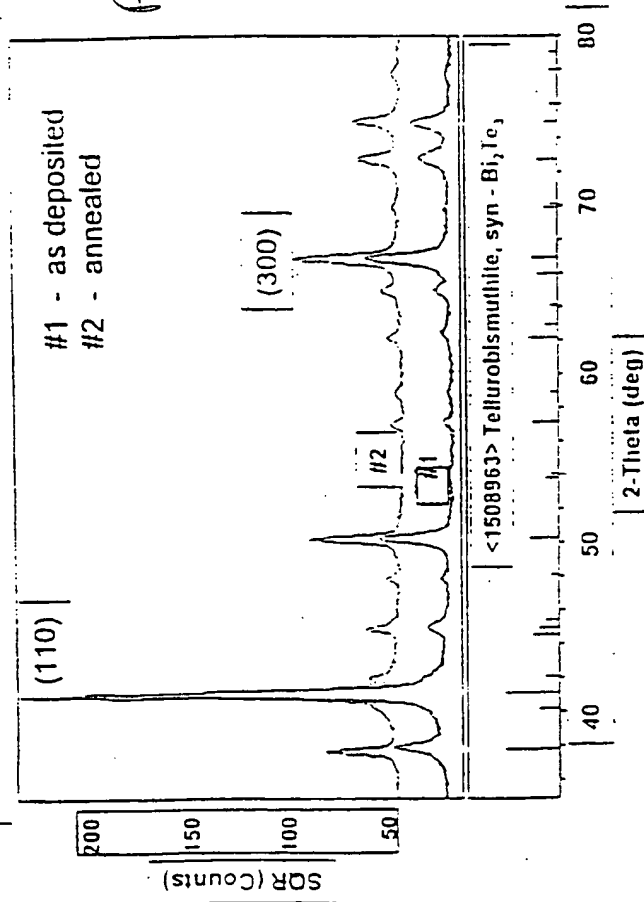
Influence of Electrolyte Concentrations on Film Stoichiometry

12



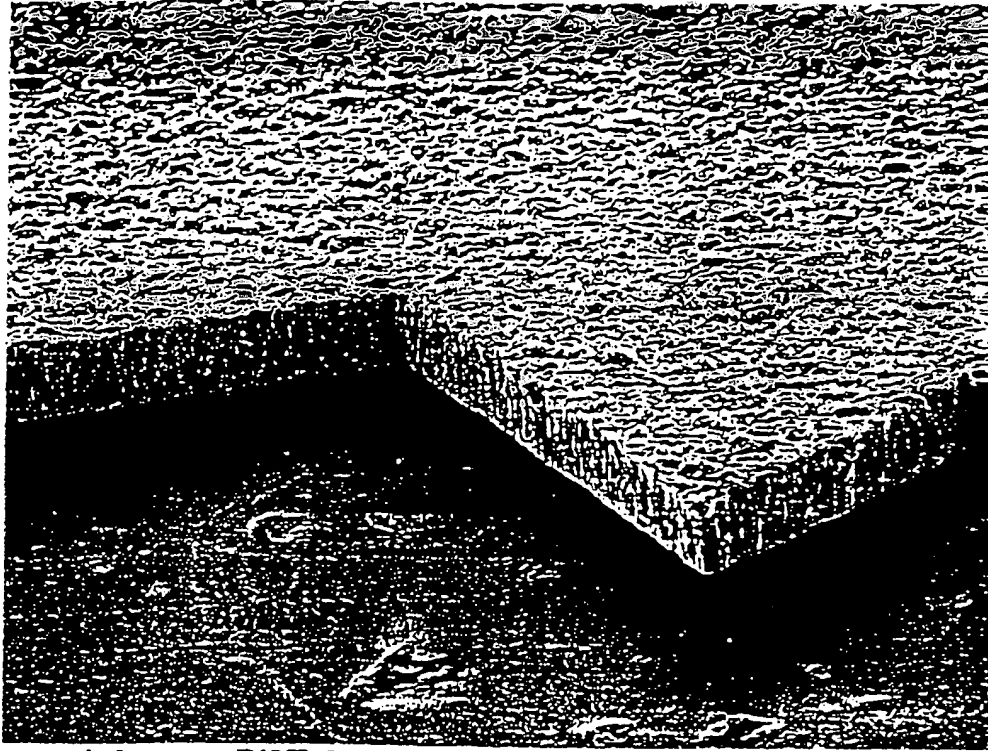
JCT99 Nagoya Trade & Industry Center

Slide 15

XRD of Electrochemically Deposited Bi_2Te_3 

LJQC/SII Review May 1998

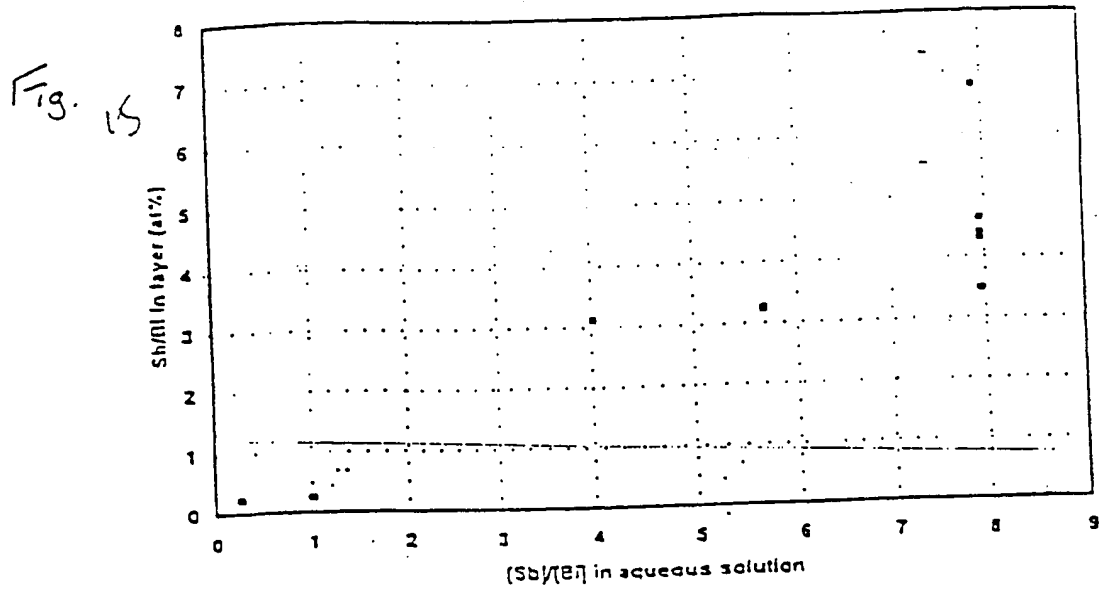
Slide 23



annealed n-type Bi₂Te₃

FIG 14

1654



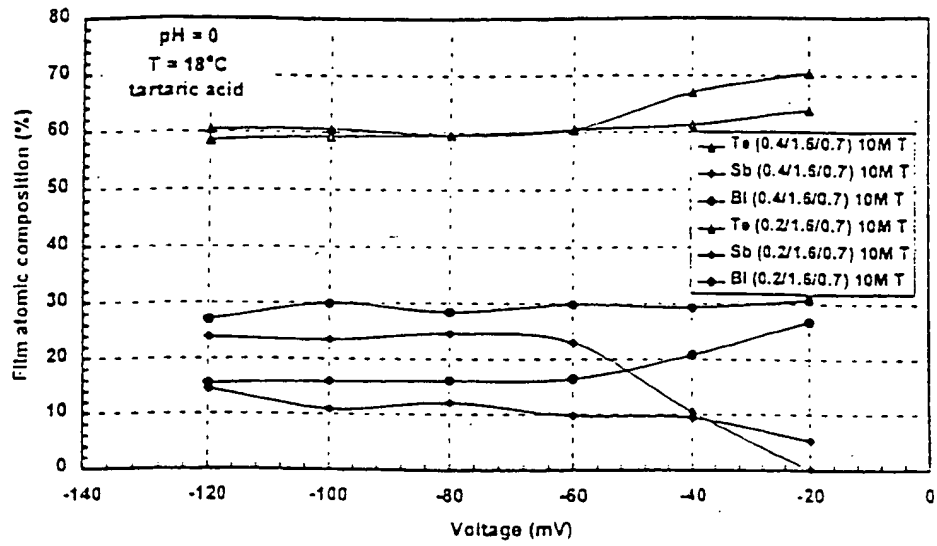


Figure: $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_3$ film composition as a function of deposition voltage for two different electrolytes (electrolyte concentrations reported as $[\text{Bi}]/[\text{Sb}]/[\text{Te}]$).

Fig 16

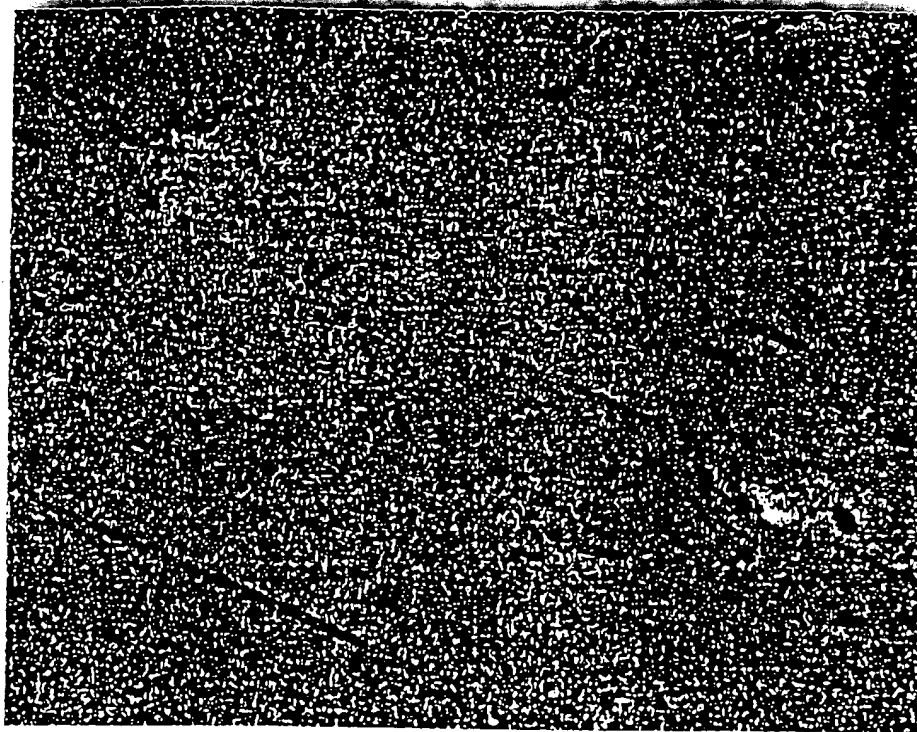


FIG 17

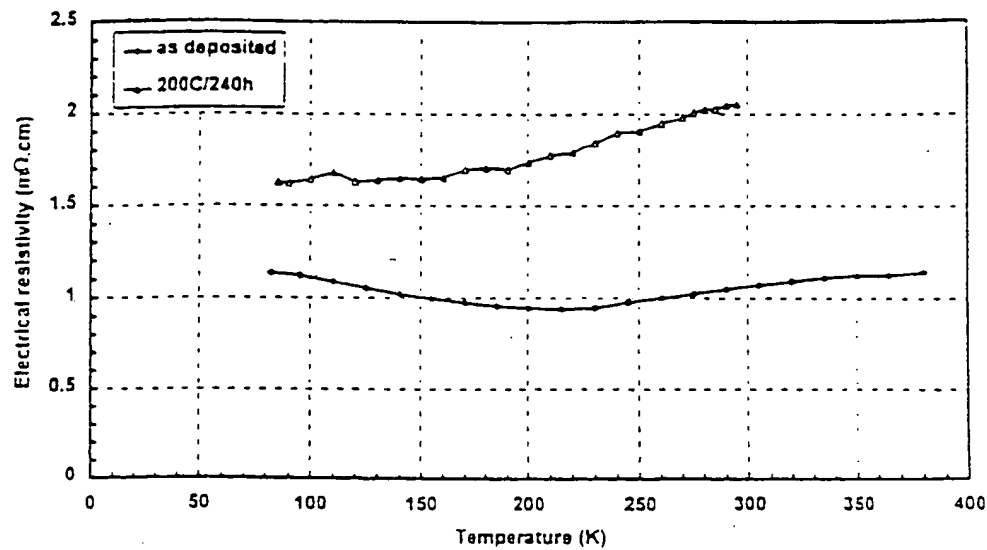


Figure: Electrical resistivity as a function of temperature (measured in the plane, parallel to the c axis of the hexagonal Bi_2Te_3 unit cell) for n-type Bi_2Te_3 films.

FIG 18

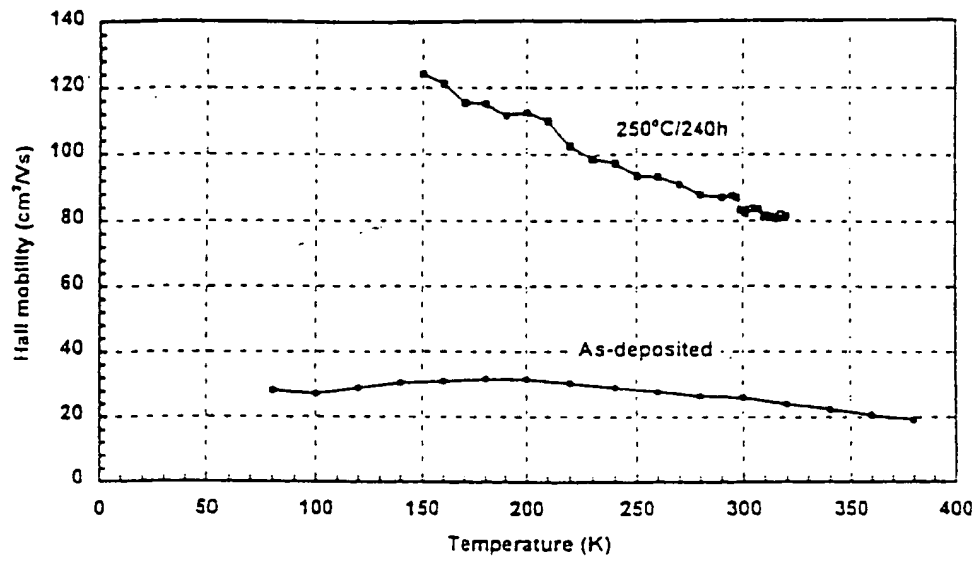
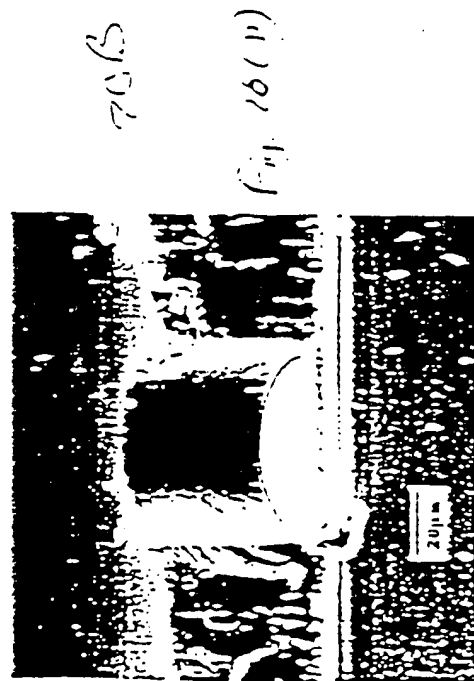
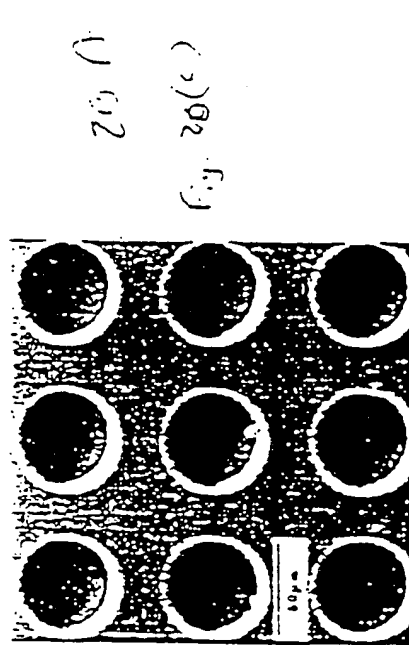
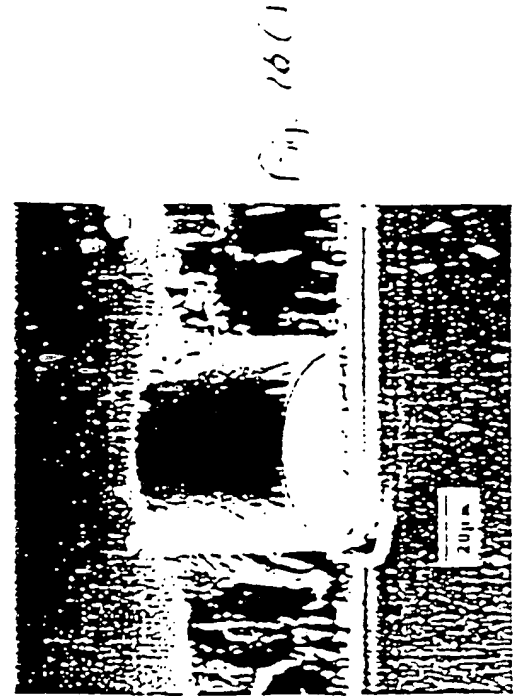
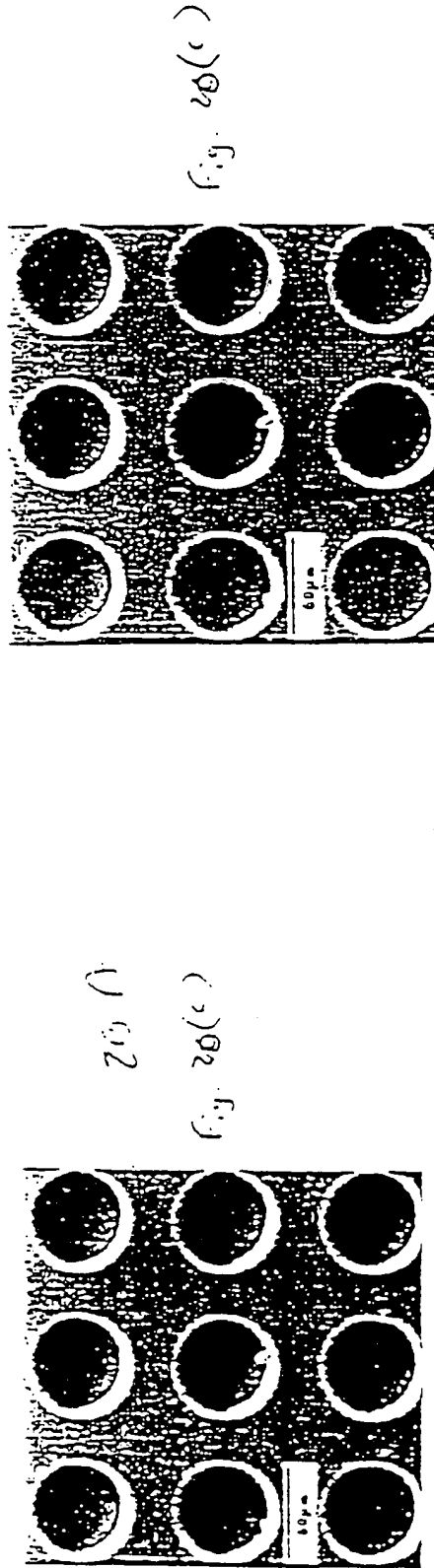


Figure: Carrier mobility as a function of temperature (measured in the plane, parallel to the c axis of the hexagonal Bi_2Te_3 unit cell) for n-type Bi_2Te_3 films.

FIG 19

Fig. 20 Thick Photoresist Deposition and Patterning



JPL

Bi₂Te₃ Electrochemical Deposition in Patterned Photoresist Layer

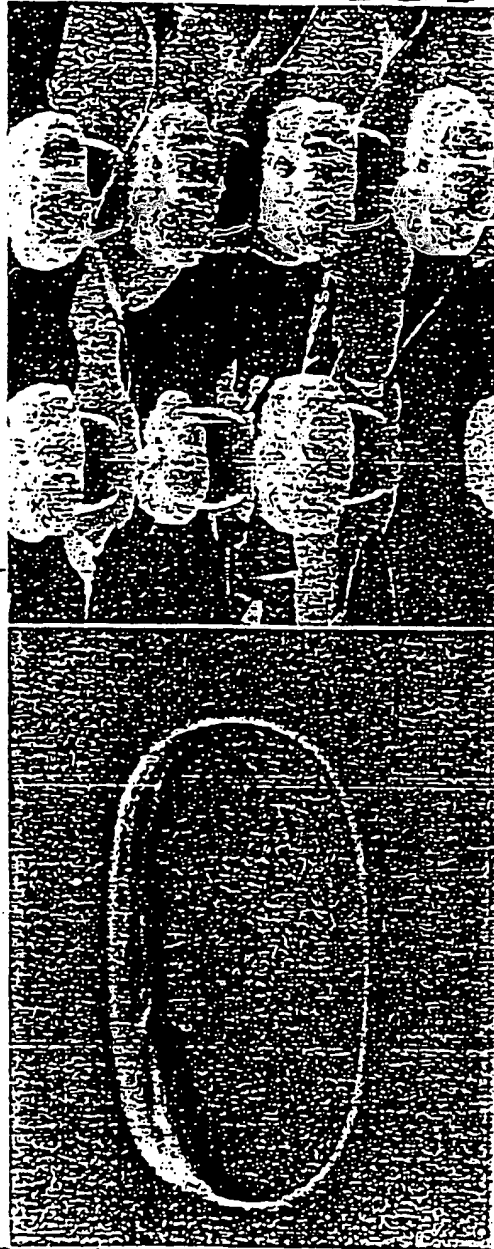


Fig 21

Slide 57

LJQC/SII Review May 1998

JPL

Bi₂Te₃ Electrochemical Deposition in Patterned Photoresist Layer (continued)

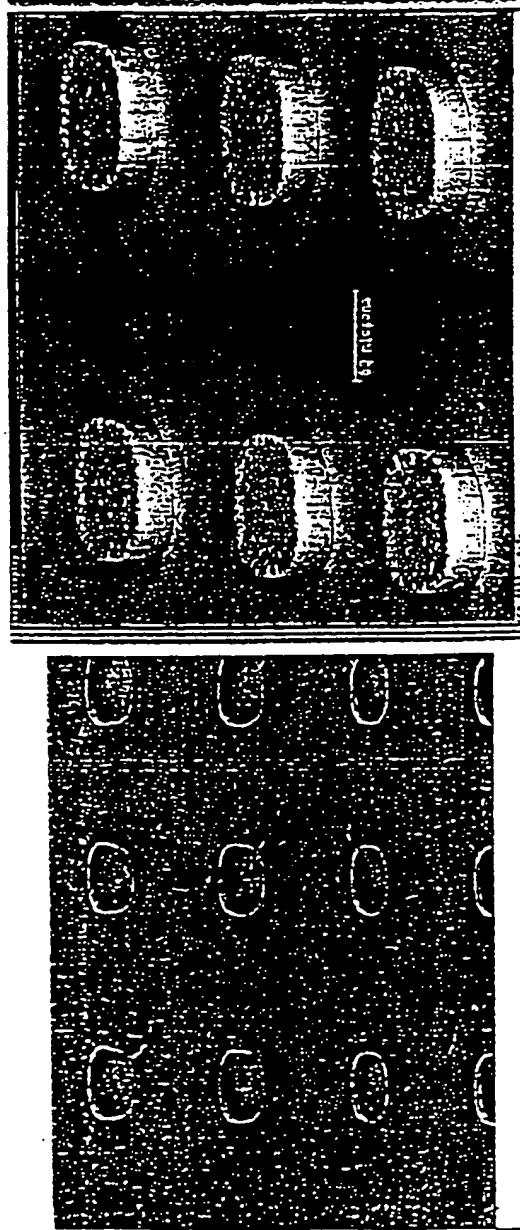
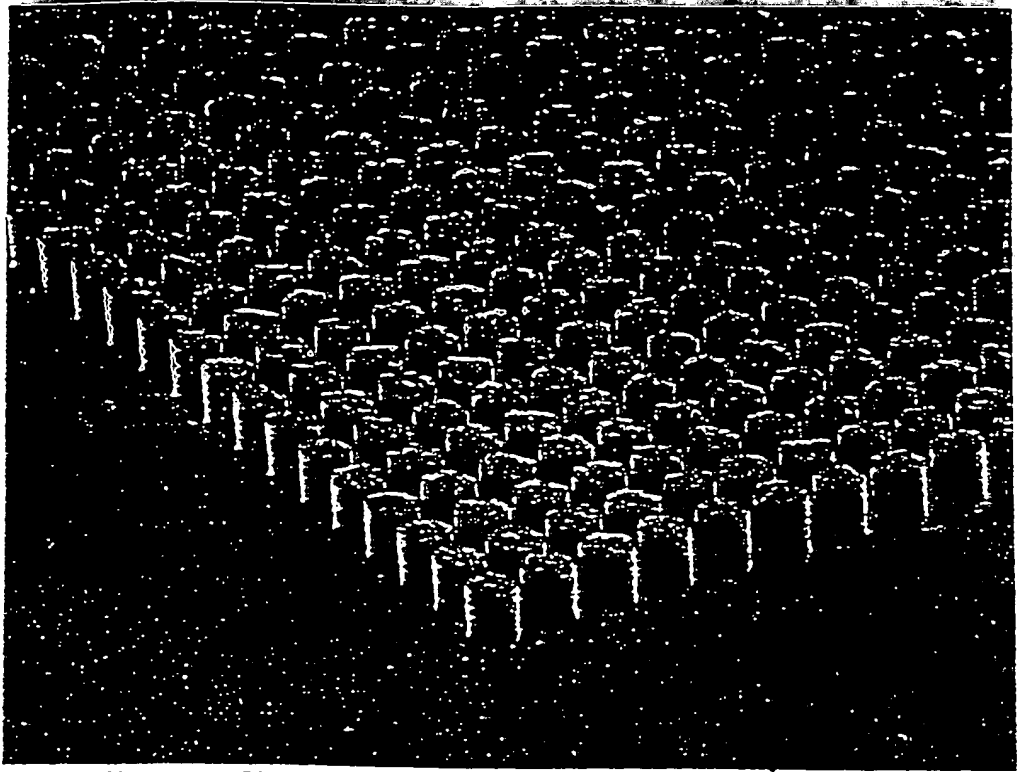


Fig. 22A

LJQC/SII Review May 1998



20 μm diameter, 50 μm tall legs (11,000 legs in $3 \times 3 \text{ mm}^2$ area)

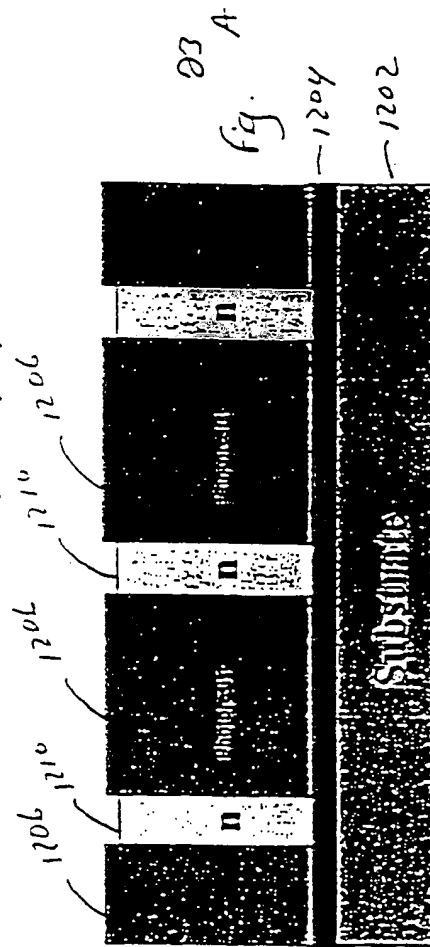
F/G 223

TE Microdevice Fabrication Steps (1)

Electrochemical deposition of

n-type Bi_2Te_3

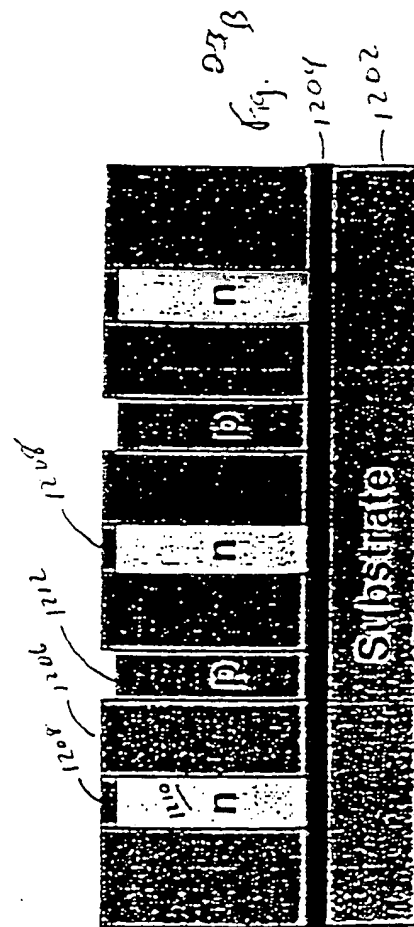
- On metallized and patterned substrate
- Thick photoresist ($\sim 40 \mu\text{m}$)
- Patterning
- Deposition of n-type legs



Electrochemical deposition of

p-type $(\text{Bi}_{1-x}\text{Sb}_x)_2\text{Te}_3$

- Masking photoresist layer to cover n-type legs
- Photomask shifted using aligner
- Patterning
- Deposition of p-type legs

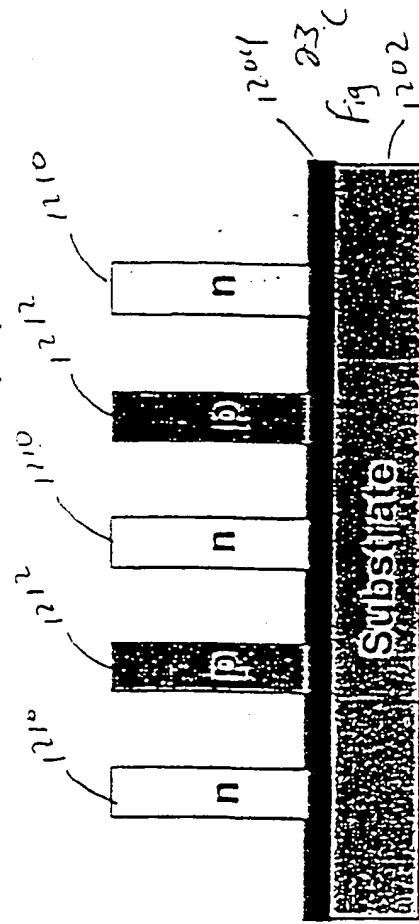


TE Microdevice Fabrication Steps (2)

Heat-treatment of

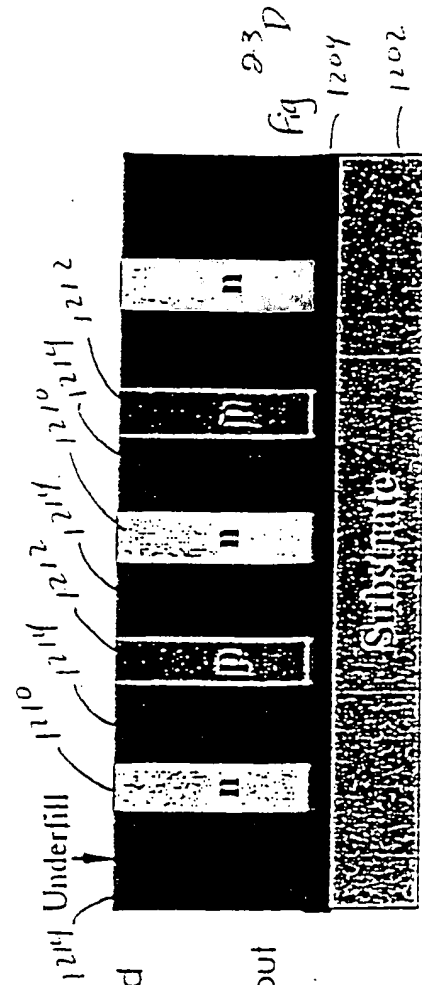
thermoelectric materials

- Dissolve photoresist
- Heat-treatment (>200°C/few hours)



Device consolidation

- Using underfill material developed for flip chip technology
- Requires curing (~150°C/30 min)
- Allows for further processing without losing mechanical integrity
 - Chemical-mechanical polishing may be needed



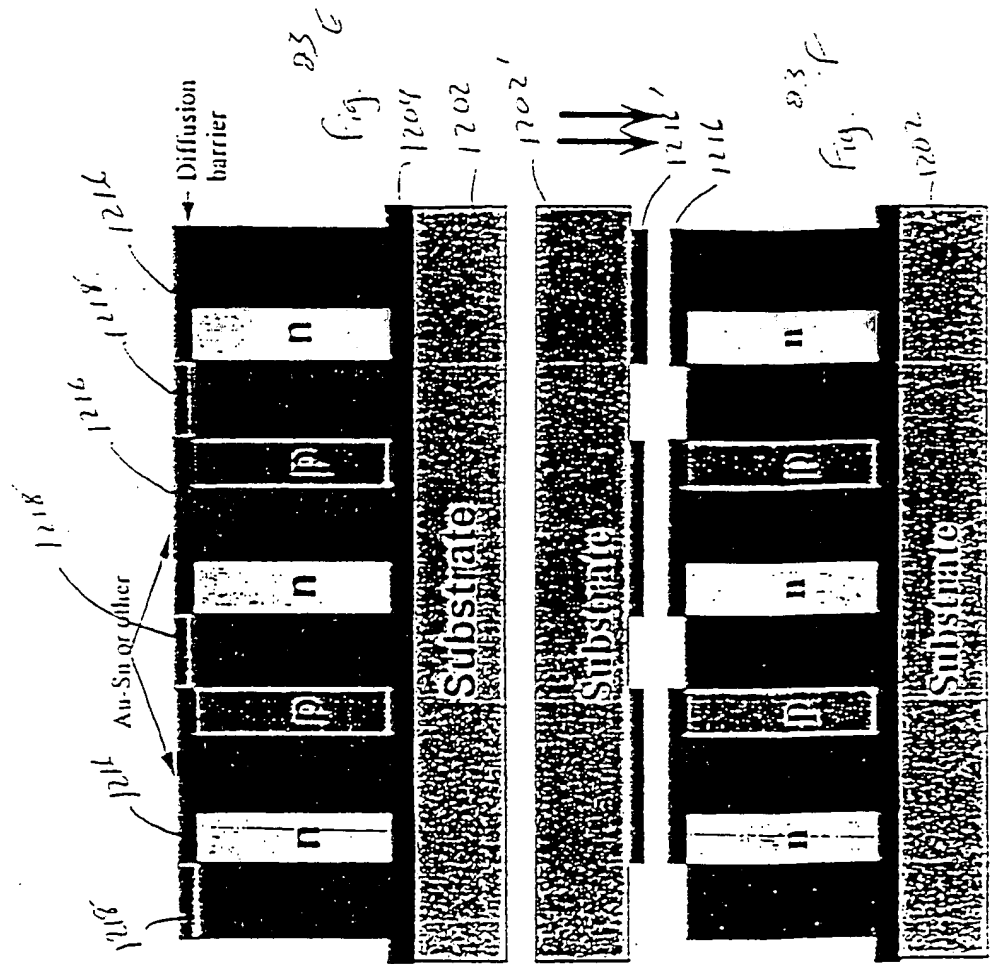
TE Microdevice Fabrication Steps (3)

Top Metallization

- New photomask applied
- Deposition of diffusion barrier, electrode material and bonding layer
- Dissolve photoresist

Top substrate bonding

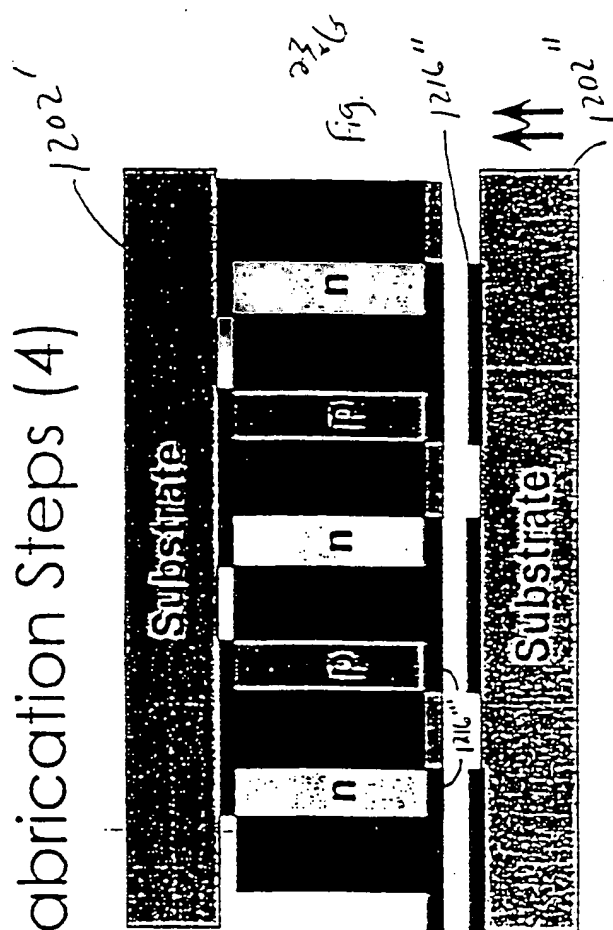
- Prepare patterned substrate
- Align substrate and thermoelectric leg bridges
- Bonding (using bonder-aligner with brief heat-treatment)
 - precision: 5 μm
 - time: 3 minutes to 300°C and 7 minutes down to 100°C



TE Microdevice Fabrication Steps (4)

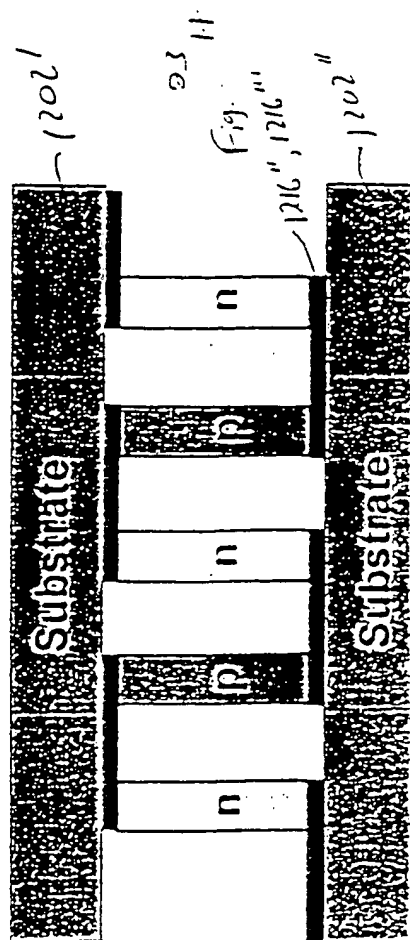
Bottom metallization

- New photomask applied
- Deposition of diffusion barrier, electrode material and bonding layer
- Dissolve photoresist



Bottom substrate bonding

- Prepare patterned substrate
- Align substrate and thermoelectric leg bridges
- Bonding (using bonder-aligner with brief heat-treatment)
- Dissolve underfill material
 - Option: leave underfill material to retain very high ruggedness



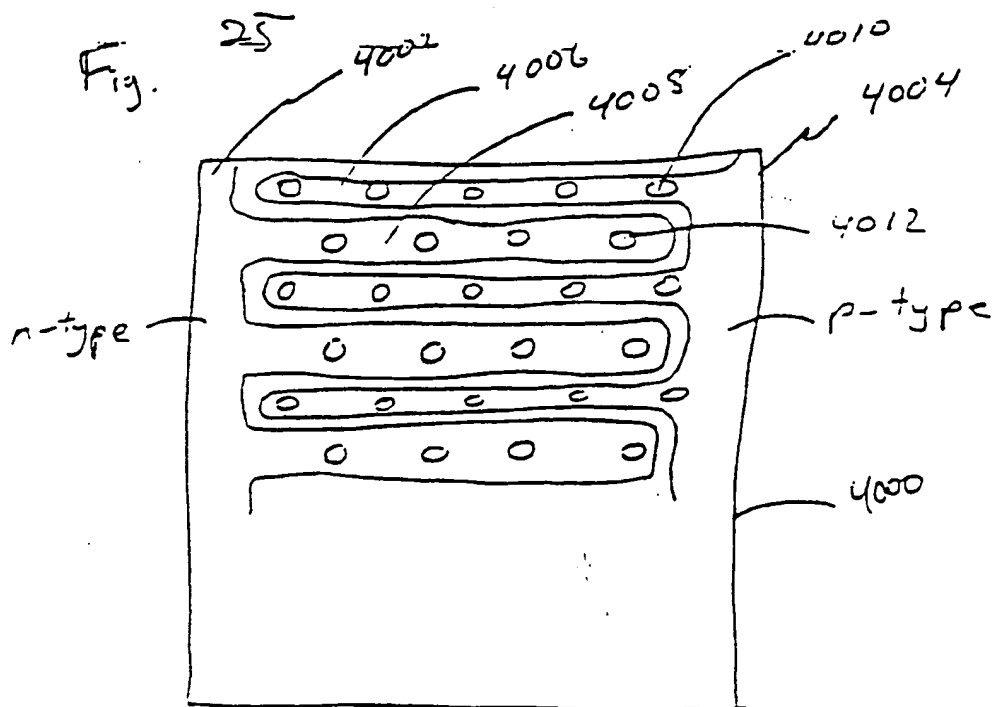
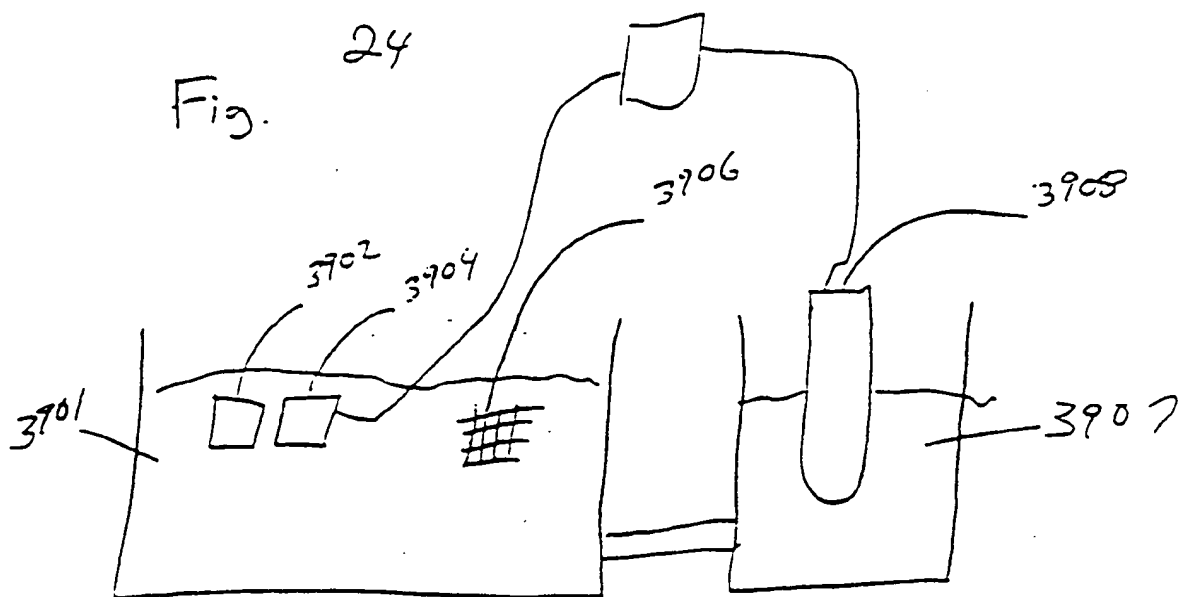
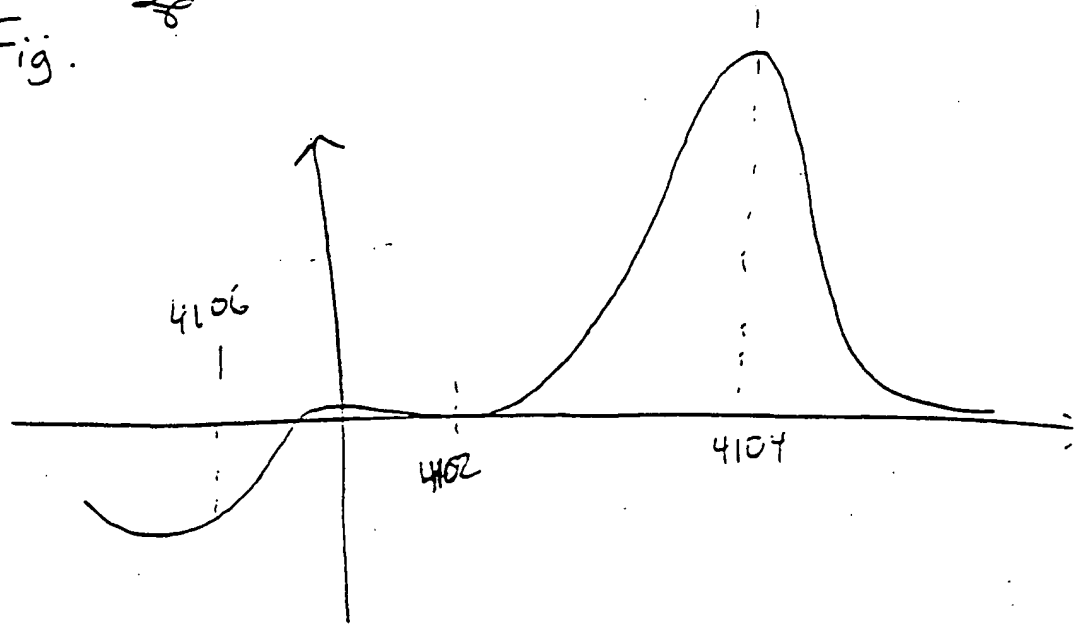
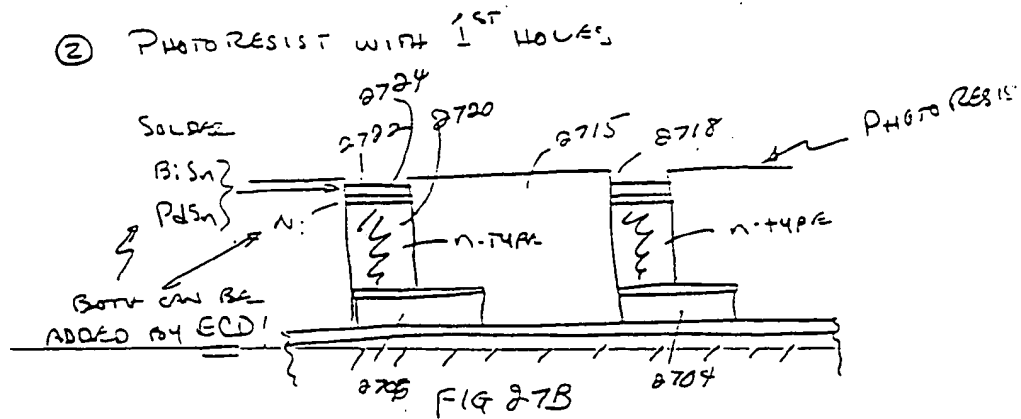
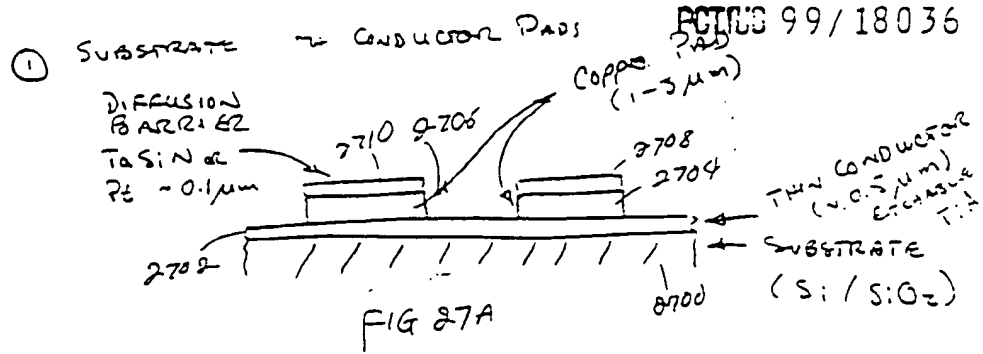
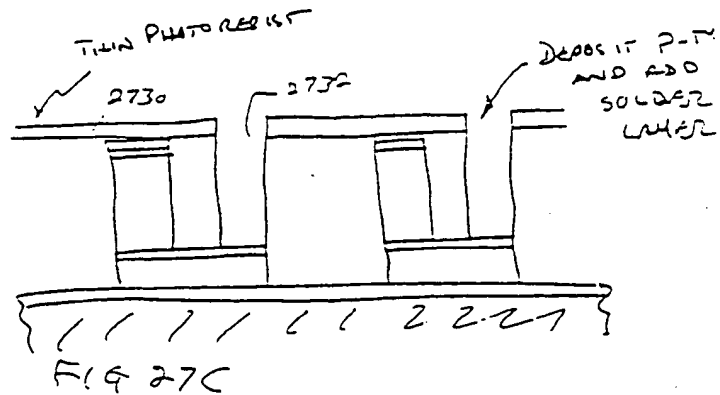


Fig. 28





- ③ ADD THE PHOTORESIST LAYER AND EXPOSE P-14
(DONE UNDER YELLOW LIGHT AS JPL HAS DONE)



D) DISSOLVE PHOTORESIST AND ETCH INITIAL METALLIZATION

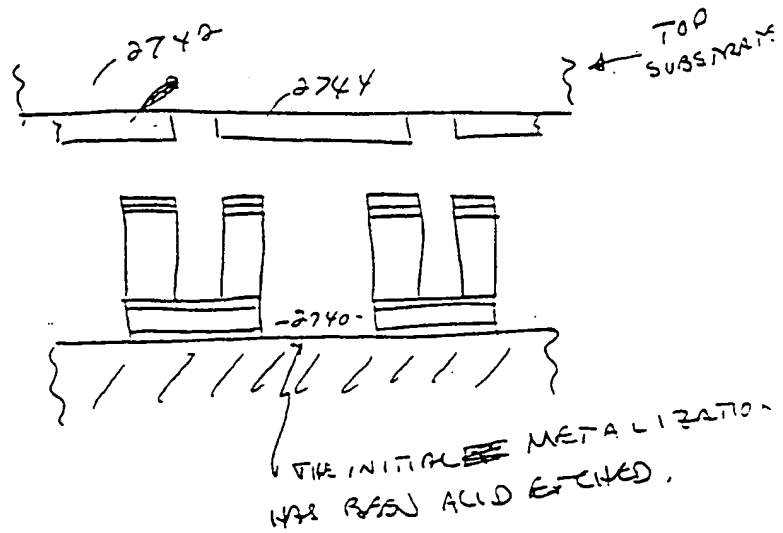


FIG. 27D

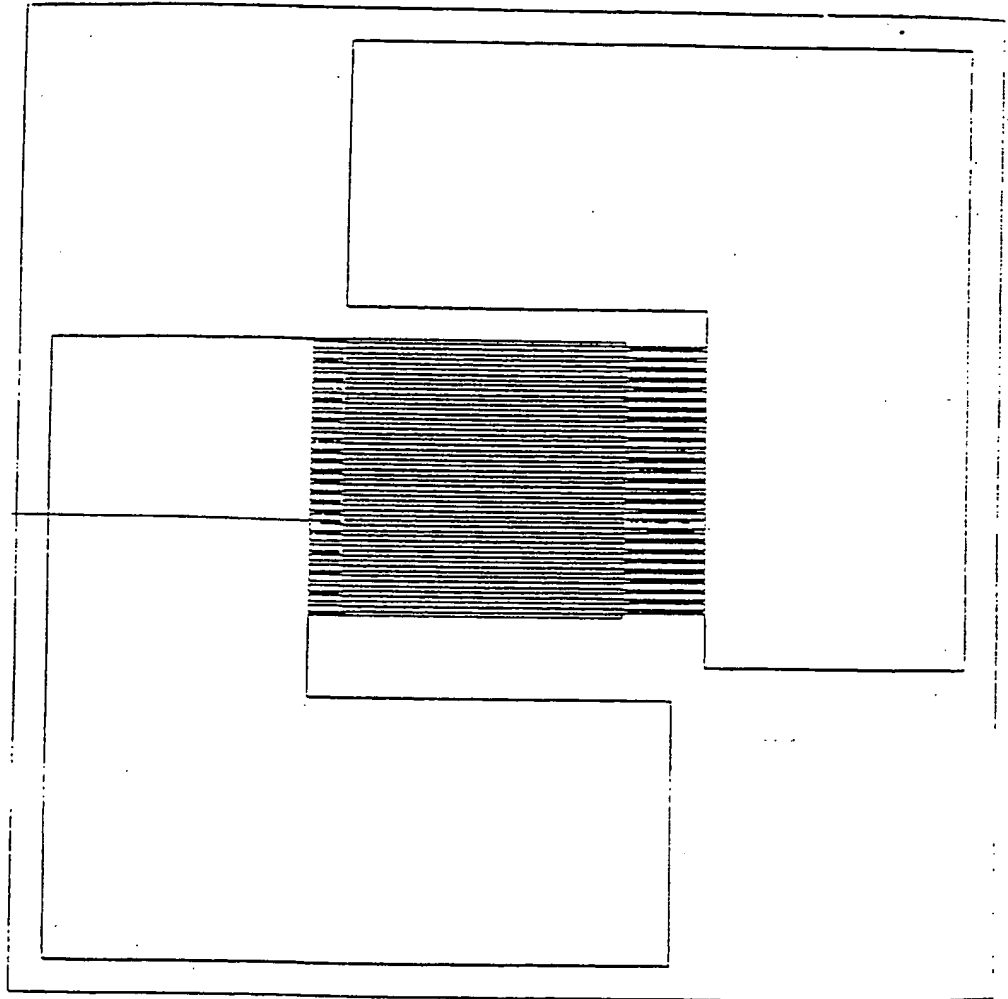


Fig 28B

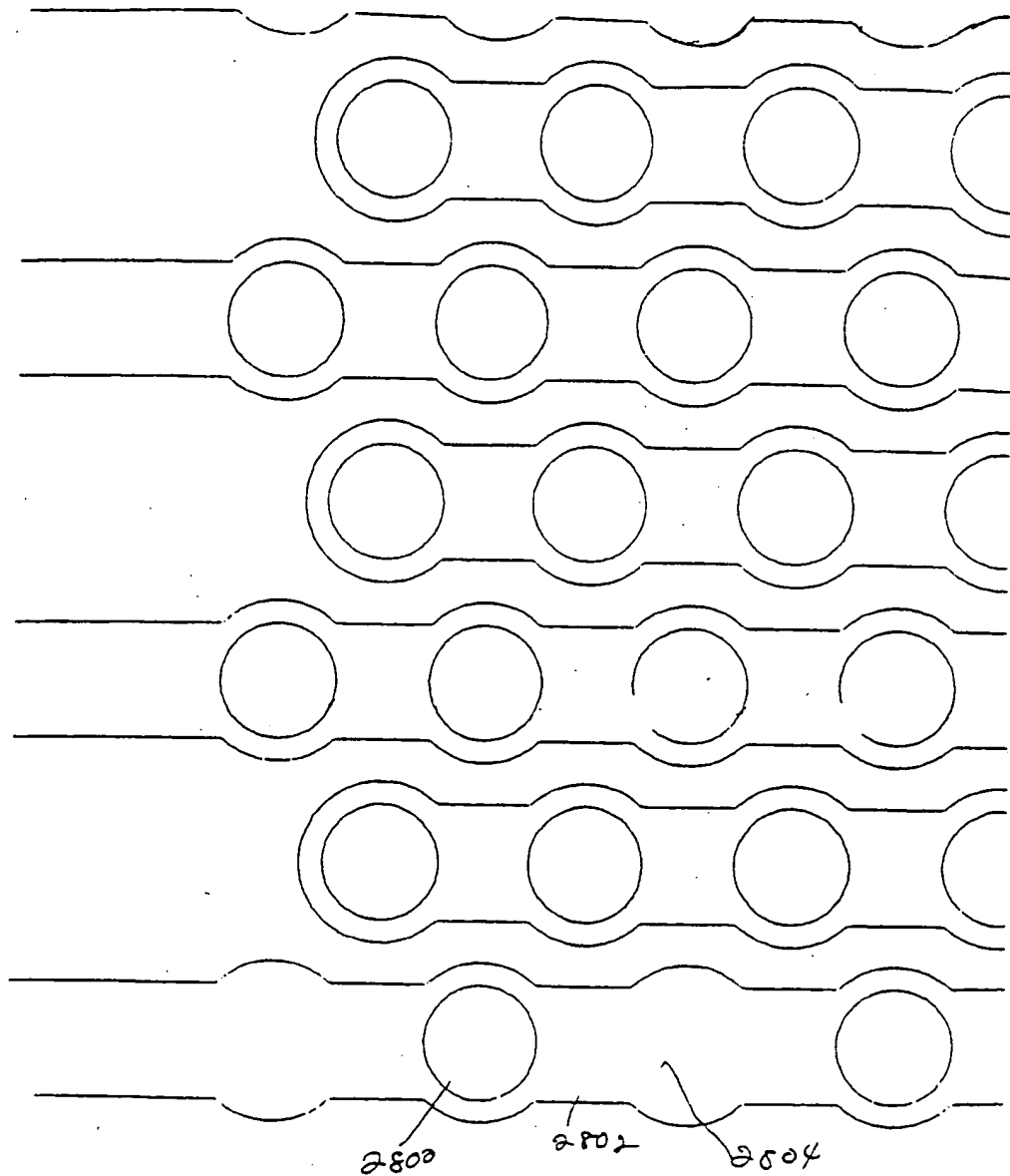


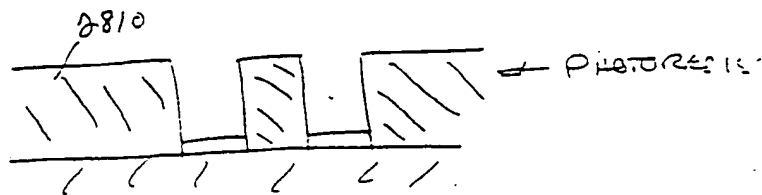
FIG 28C

INTERDIGITATED SEQUENCE

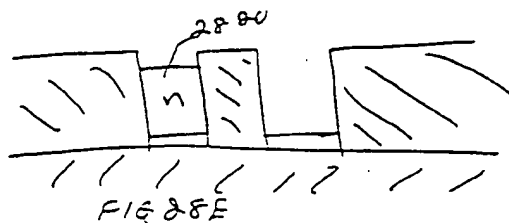
- 1) SUBSTRATE WITH FINGERS (MEMS) ← MEMS FINGERS
SUBSTRATE

FIG 28A

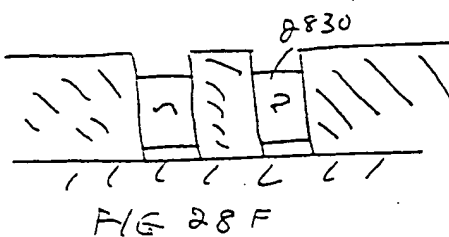
- 2) PHOTORESIST WITH "HOLES" IS ADDED



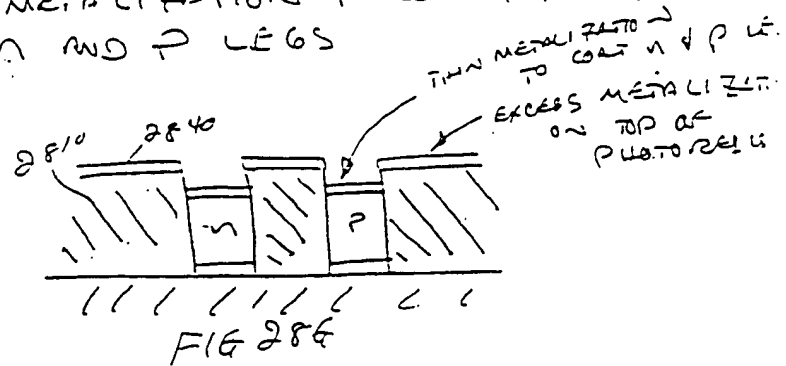
- 3) N-TYPE ECD IN N-TYPE ELECTROLYTE
(P-TYPE FINGERS ARE BIASED POSITIVE
TO PREVENT DEPOSITION)



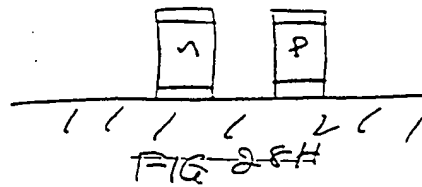
- 4) P-TYPE ECD IN P-TYPE ELECTROLYTE
(N-TYPE ELECTRODES BIASED POSITIVE
TO PREVENT DEPOSITION)



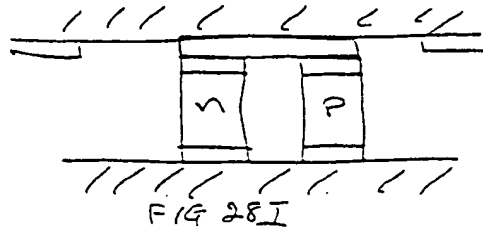
- 5) THIN METALIZATION TO CO TOPS OF
N AND P LEGS



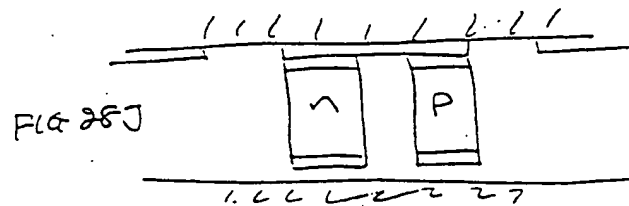
- 6) PHOTORESIST DISSOLVED (REMOVED)



- 7) TOP SUBSTRATE WITH INTERCONNECT BUS ATTACHED TO LEGS



- 8) BOTTOM SUBSTRATE REMOVED



- 9) New Bottom Substrate with Interconnect
Buses Bonded to Legs

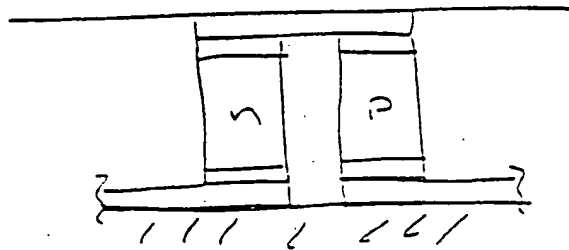


FIG 28K

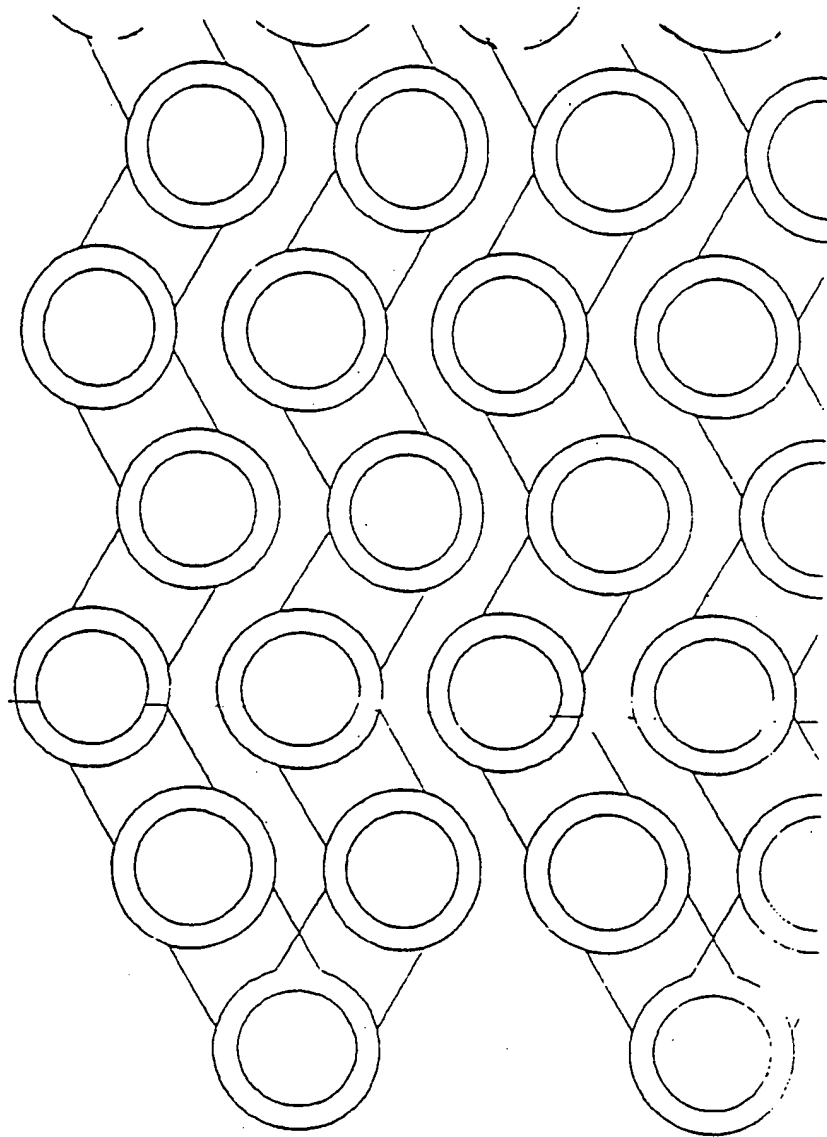


FIG 28L

INTERNATIONAL SEARCH REPORT

International application No
PCT/US99/18036

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : HO1L 35/34, 35/28, 35/30, 35/16, 35/20, 21/20; C04B 35/00

US CL : 136/201, 203, 205, 238, 240; 205/157; 252/62.3T; 438/54

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 136/201, 203, 205, 238, 240; 205/157; 252/62.3T; 438/54

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X — Y	US 5,712,448 A (VANDERSANDE et al) 27 January 1998, col. 5, line 64 through col. 9, line 40.	1-16, 23, 24, 78, 83 <hr/> 1, 7
Y	US 5,517,468 A (INOUE et al) 14 May 1996, col. 3, lines 1-60; Fig. 1; col. 4, line 49 through col. 4, line 54; and, Fig. 6.	1, 7
X	KACSICH et al. Films of Ni-7 at% V, Pd, Pt and Ta-Si-N as diffusion barriers for copper on Bi Te J. Phys. D: Appl. Phys. April 1998. Vol. 31. pages 2406-2411.	23, 24

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

A	document defining the general state of the art which is not considered to be of particular relevance	*T*	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
B	earlier document published on or after the international filing date	*X*	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
L	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*Y*	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
O	document referring to an oral disclosure, use, exhibition or other means	*Z*	document member of the same patent family
P	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

22 OCTOBER 1999

Date of mailing of the international search report

17 NOV 1999

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

THOMAS PARSONS *Thomas Parsons*
Telephone No. (703) 308-0661

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/18036

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A --- X	FLEURIAL et al. Thermoelectric Microcoolers for Thermal Management Applications Proceedings of the XVI International Conference on Thermoelectrics August 1997.	17-22, 29-36 ----- 25,27
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A	US 4,909,857 A (ONDRIS et al) 20 March 1990, entire document.	38-42, 43-56, 62, 64-66, 69, 73
--	--	--
A --- X	US 5,362,983 A (YAMAMURA et al) 08 November 1994, entire document.	67-68, 70-72, 74 ----- 75-77 -----

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US99/18036

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 37, 57-61, 63, 79-82
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

Please See Extra Sheet.

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US99/18036

B. FIELDS SEARCHED

Electronic data bases consulted (Name of data base and where practicable terms used):

WEST

search terms: electrochemical deposition, thermoelectric, timepiece, wristwatch, bismuth, antimony, tellurium, reference, counter, film

BOX I. OBSERVATIONS WHERE CLAIMS WERE FOUND UNSEARCHABLE

2. Where no meaningful search could be carried out, specifically:

Claims 37, 57, 79, 80, 81 and 82 could not be searched because they are method claims dependent upon an apparatus claim.

Claims 58-59 could not be search because they appear to be missing.

Claims 60, 61 and 63 could not be searched because they are dependent upon the missing claims.

PATENTEC OPTICALS

PATENT ZAP Request

Rqx: 104180

@IBM

PAT BOYKIN

CAS SALY - AUSTIN

WO 00/08693

Date: 4/6/00
Time: 11:13:23 AM
Req. Date:
Req. Time:

--Stapled